EXHIBIT A

DOCKET NO.: 1745950-00120US2
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.
Petitioner

v.

THE TRUSTEES OF PURDUE UNIVERSITY
Patent Owner

IPR2022-00309
U.S. Patent No. 8,035,112

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,035,112 CHALLENGING CLAIMS 1, 6, 7, and 10–12 UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104

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STMicroelectronics, Inc. ("Petitioner") respectfully requests *inter partes* review ("IPR") of claims 1, 6, 7, and 10–12 of U.S. Patent No. 8,035,112 (the "'112 patent") (EX1001) pursuant to 35 U.S.C. §§ 311–19 and 37 C.F.R. § 42.1 *et seq.*

I. INTRODUCTION

Titled "SIC power DMOSFET with self-aligned source contact," the '112 patent is directed to metal oxide semiconductor field effect transistors (MOSFETs) that have self-aligned source contacts. The problem described by the '112 patent and its alleged solution, however, were well-known in the art, as detailed in the grounds below.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner STMicroelectronics, Inc. ("ST") is a real party-in-interest. Although STMicroelectronics N.V., ST's parent company, and STMicroelectronics International N.V., which is under common ownership with ST, are not real parties-in-interest under the governing legal standard for making that determination, ST identifies them as real parties-in-interest for purposes of this Petition to avoid any disputes over that issue.

B. Related Matters

According to USPTO records, the '112 patent is owned by The Trustees of Purdue University ("Patent Owner" or "PO"). Petitioner knows of the following co-

pending litigations involving the '112 patent: *The Trustees of Purdue University v. STMicroelectronics N.V. and STMicroelectronics, Inc.*, No. 6:21-CV-00727 (W.D. Tex.) and *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 1:21-CV-840 (M.D.N.C.). The earliest date of service on Petitioner in the co-pending litigation was July 20, 2021.

C. Counsel

Under 37 C.F.R. §§ 42.8(b)(3)–(4), Petitioner identifies the following lead and backup counsel, to whom all correspondence should be directed.

Lead Counsel:	Richard Goldenberg (Reg. No. 38,895)
Backup Counsel:	Gregory Lantier (*pro hac vice* to be filed)
	Scott Bertulli (Reg. No. 75,886)
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Petitioner consents to service by e-mail on lead and backup counsel.

III. LEVEL OF ORDINARY SKILL

A person of ordinary skill in the art ("POSITA") at the time of the earliest claimed priority date of the '112 patent (April 23, 2008) would have had the equivalent of a Bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices. Less work experience may be compensated by a higher level of education, such as a Master's Degree, and vice versa. EX1002, ¶23.

IV. CERTIFICATION OF GROUNDS FOR STANDING

Petitioner certifies under 37 C.F.R. § 42.104(a) that the patent for which review is sought is available for *inter partes* review (IPR) and under 37 C.F.R. §§ 42.101(a)–(c) that Petitioner is not barred or estopped from requesting an IPR challenging the patent claims on the grounds identified in this Petition.

V. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED

A. Claims for Which Review is Requested and Grounds on Which the Challenge is Based

Under 37 C.F.R. §§ 42.22(a)(1) and 42.104(b)(1)–(2), Petitioner requests cancellation of claims 1, 6, 7, and 10–12 of the '112 patent on the following grounds:

Ground	References	Basis	Claims Challenged
I	*Ueno*	§ 103	1, 6, 7, 10, 12
II	*Ueno* in view of *Lidow*	§ 103	11

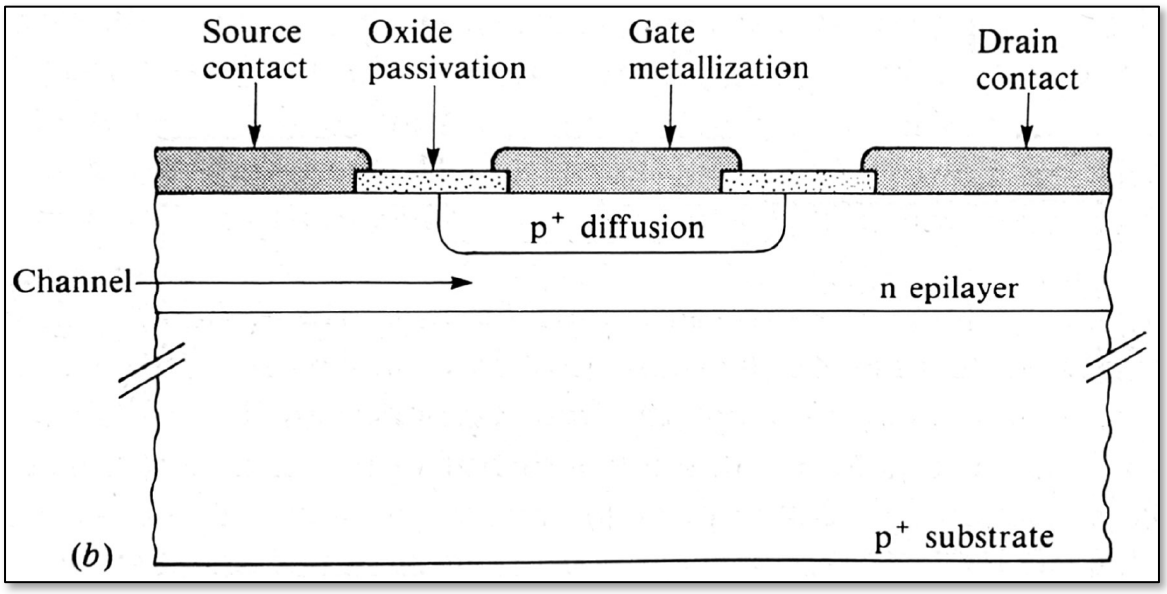
This Petition, supported by the declaration of Dr. Subramanian (EX1002), demonstrates that there is a reasonable likelihood Petitioner will prevail with respect to cancellation of at least one of the challenged claims. *See* 35 U.S.C. § 314(a).

VI. TECHNOLOGY BACKGROUND

A. Field-Effect Transistor ("FET")

A field-effect transistor ("FET") is a type of transistor that uses an electric field to control the flow of current in a semiconductor. *See* "Power MOSFETs – Theory and Applications," Duncan A. Grant and John Gowar, 1989 ("*Grant*") (EX1009) at 1 ("The metal-oxide-semiconductor field-effect transistor (MOSFET) is the most commonly used active device in the very large-scale integration of digital integrated circuits …. The conductance of a piece of semiconductor depends on the number of free carriers it contains and on their mobility. The effective number of free carriers can be modified by establishing a static electric field in the semiconductor in the direction transverse to the current flow."). A FET generally includes a source, a drain, and a gate, as *Grant* illustrates in a cross section of a

junction field-effect transistor (JFET) in Figure 1.1, reproduced below. *See, e.g.*, EX1009, 2, Figure 1.1. EX1002, ¶24.



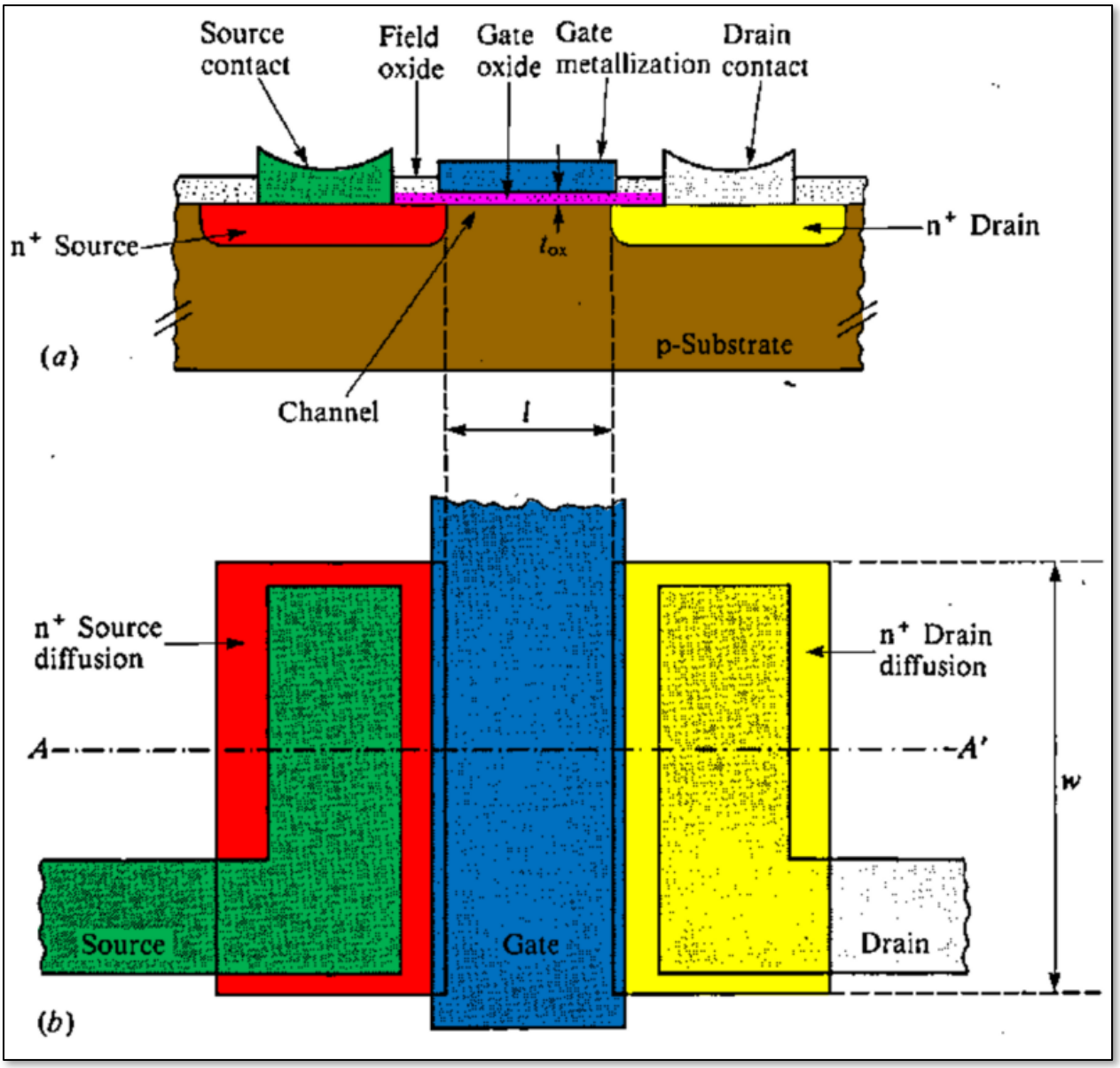
EX1009, Figure 1.1

The flow of current is controlled by applying a voltage to the gate (thereby creating an electric field), which in turn alters the conductivity of the channel formed between the drain and the source. *Id.* at 3. In this structure, the current moves horizontally between the source and drain. EX1002, ¶25

Grant notes that "[t]he successful manufacture of the JFET depended on the introduction of *planar* silicon technology in 1960" that involves a "combination of processes," including epitaxial crystal growth, photolithographic etching of windows in the oxide layer, and introduction of controlled levels of impurity (*i.e.*,

doping) into selected regions of the silicon by diffusion or implantation. EX1009, 3. EX1002, ¶26.

"Further technological refinements in the early 1960s enabled a different type of field-effect transistor to be made. This was the metal-oxide-semiconductor field-effect transistor (MOSFET)." EX1009, 5. *Grant* points out that the difference between a JFET and a MOSFET is "[t]he controlling gate electrode is now separated from the semiconductor by a thin insulating layer of gate oxide, as shown in Figure 1.3." *Id.*; *see also* U.S. Patent No. 5,233,215 ("*Baliga*") (EX1004), 1:45–50. In Figure 1.3 (reproduced below), *Grant* illustrates a cross section and a plan view of a MOSFET. EX1009, 5. When the MOSFET is turned on, current can flow between the source and drain through the channel, shown in the figure and formed in the p-type substrate. The source region is annotated in red, the drain region in yellow, the p-type substrate in brown, the gate in blue, the gate oxide in magenta, and the source contact in green. The source contact is often referred to as "source metallization," "source metal," or "source electrode." *See* EX1009, 15–16, Figures 1.12 and 1.13 (illustrating the source metallization); EX1013, Figure 1, 1:38 ("source metal"); EX1004, 2:64 ("source electrode"). EX1002, ¶27.



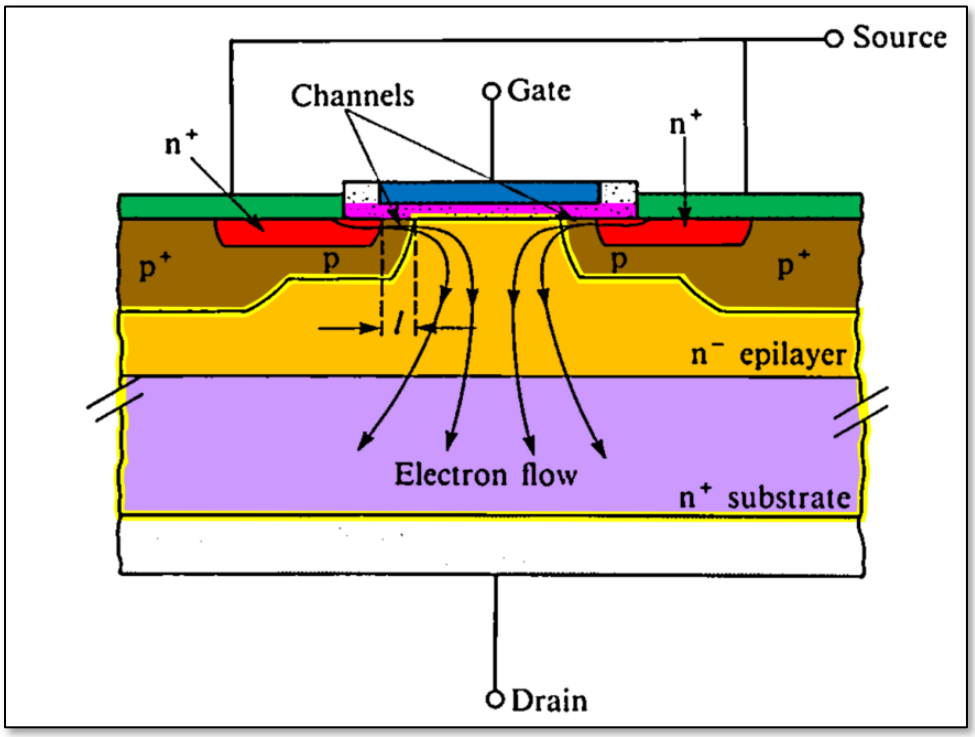
EX1009, Figure 1.3 (annotated)

B. Power MOSFET

The MOSFET became "important in devices designed for power applications." EX1009, 5; *see also* EX1004, 2:14–16. *Grant* notes that "the decision as to what constitutes a power device is quite arbitrary" and the term is applied to

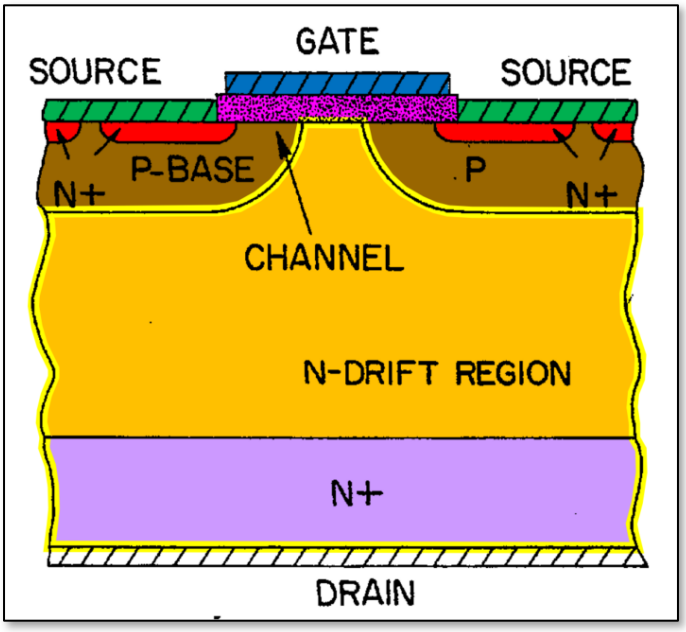
"any device capable of switching at least 1 A" (*i.e.*, turning on and off a current of 1 ampere flowing from the drain to the source). EX1009, 5–6. EX1002, ¶28.

Grant further notes that "the planar structure of Figure 1.3 is unsatisfactory if it is simply scaled up for higher powers." EX1009, 8. "[T]he drain-source spacing has to be increased in order to obtain a high voltage blocking capability." *Id.* One solution well known in the art was to change from the lateral structure as illustrated in *Grant*'s Figure 1.3 to a vertical structure that uses the substrate material to form the drain region such that "the current flows 'vertically' through the silicon from drain to source." *Id.* This change led to the ***vertical double-diffused MOSFET***, which *Grant* illustrates in Figure 1.11. *Id.* at 13–14, Figure 1.11. EX1002, ¶29.



EX1009, Figure 1.11 (annotated)

The vertical power MOSFET structure as described by *Grant* is well known. For example, *Baliga* also illustrates a vertical double-diffused MOSFET in Figure 1, which is reproduced below. EX1004, 6:12–13 ("FIG. 1 is a cross-sectional view of a known DMOSFET device"). EX1002, ¶30.



EX1004, FIG. 1 (annotated)

The term "double-diffused" derives from a manufacturing technique commonly used to form the n+ source regions within the p-type body region: "[t]he p-type 'body' region, in which the channel is formed when a sufficiently positive gate voltage is applied, and the n+ source contact regions are diffused successively through the same window etched in the oxide layer." EX1009, 14; *see also* EX1004, 2:35–38. The p-type body region is often referred to as "p-type wells" or "p-base

regions." *See, e.g.*, EX1009, 146 ("p-type wells"); EX1004, 2:35 ("p-base region"), Figure 1 (illustrating p-base regions). EX1002, ¶31.

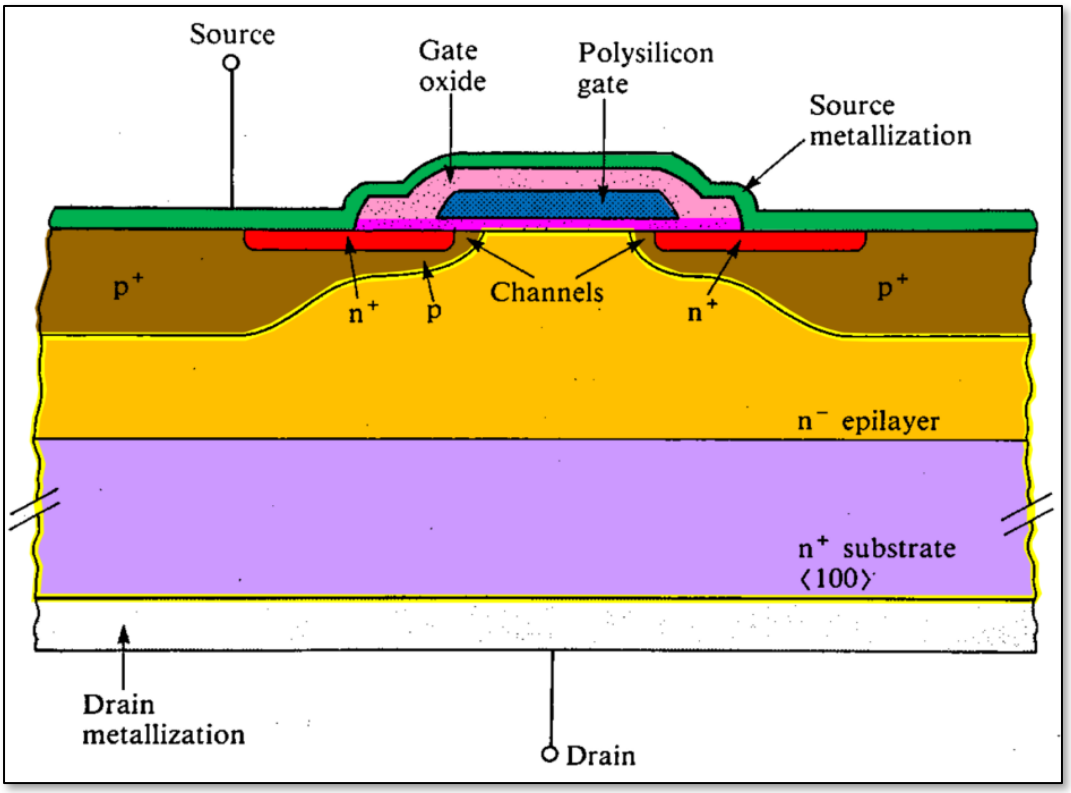
In each of the above *Grant*'s Figure 1.11 and *Baliga*'s Figure 1, the source regions are annotated in red, the p-type body regions in brown, the gate in blue, the gate oxide in magenta, and the source contacts in green. The drain region (outlined in yellow) comprises the substrate (annotated in lavender) and the epilayer (annotated in orange). Electrons flow from the source to the drain through the channels formed in the p-type wells, the epilayer, and the substrate. The epilayer is often referred to as the "drift region." *Grant* notes that "[t]he drain drift region is particularly critical to the design of a power MOSFET" because "[i]ts principal function is to block and support the full forward voltage held off by the transistor in its turned-OFF state" and "it has also to carry the full forward current in the ON state." EX1009, 74. EX1002, ¶32.

According to *Grant*:

> A development that was of great importance in integrated-circuit MOS technology in the 1970s was the ***use of heavily doped polycrystalline silicon***, rather than aluminum, ***to form the gate electrode***. It has a number of advantages for the power FET also:
>
> 1. It simplifies the connection metallization: ***an oxide layer can be formed over the poly-Si, and the***

> ***source metallization may then be extended over the whole of the upper surface***. This is shown in Figure 1.12.
>
> 2. The poly-Si layer can be deposited with great accuracy, and the gate oxide is more stable and less prone to contamination than when an aluminum gate contact is used. As a result there is better control of the threshold voltage.
>
> 3. The source is self-aligned automatically with the gate edge.

EX1009, 14–15. *Grant*'s Figure 1.12 is reproduced below with the source region annotated in red, the p-type body regions in brown, the gate in blue, the gate oxide in magenta, the oxide layer formed over the polysilicon gate in pink, and the source metallization in green. The drain region, outlined in yellow, comprises the substrate (annotated in lavender) and the epilayer (annotated in orange). As can be seen in *Grant*'s Figure 1.12, the source metallization extends over the whole of the upper surface. EX1002, ¶33.

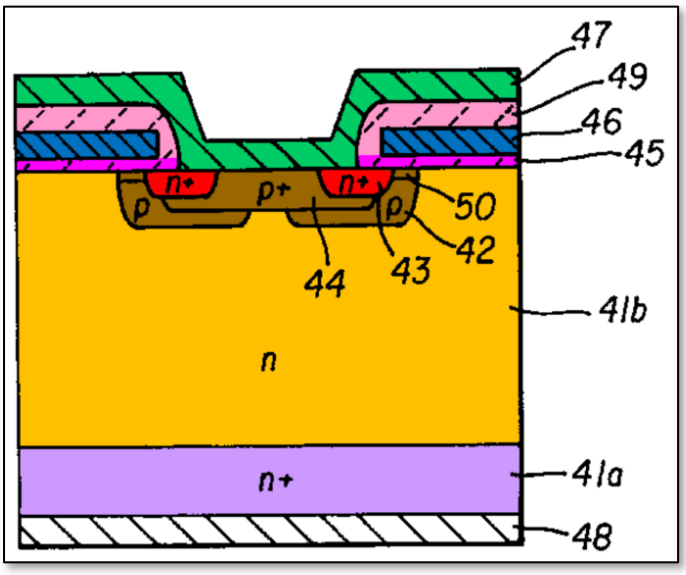


EX1009, Figure 1.12 (annotated)

C. Plurality of Cells

Prior art references conventionally illustrate a cross-sectional view of one unit cell of a power MOSFET (*e.g.*, as in *Grant*'s Figures 1.11 and 1.12 and *Baliga*'s Figure 1, all reproduced above). U.S. Patent No. 6,238,980 to Ueno ("*Ueno*") (EX1003) shows a similar example of a cross-sectional view of one unit cell of a power MOSFET in Figure 1 (reproduced below). *See* EX1003, 7:65–66. A POSITA would have appreciated that, while the unit cells of the MOSFETs in *Grant*'s Figures 1.11 and 1.12 and *Baliga*'s Figure 1 are drawn centered on their gates (annotated in blue), *Ueno* illustrates the unit cell of its MOSFET shifted one half unit so it is

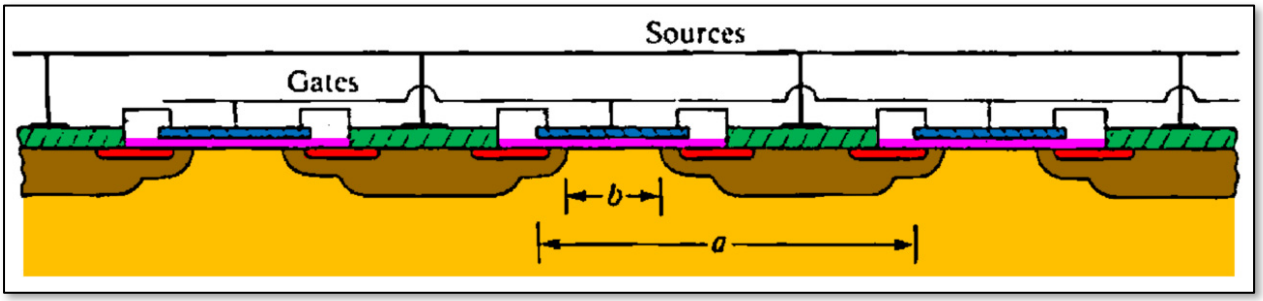
centered on its base region (annotated in brown). In this view, two gates are visible. EX1002, ¶34.



EX1003, FIG. 1 (annotated)

Regardless of how a unit cell is illustrated, a POSITA would have understood that a power MOSFET device may include a plurality of adjacent unit cells, laid out next to each other at a regular pitch. *See, e.g.*, EX1009, Figure 1.13; EX1013, Figure 1; *see also* EX1009, 383 ("A vertical diffused power MOSFET consists of many parallel cells . . ."); *id.* at 15 ("High-current capability is obtained by connecting many cells together in parallel."); EX1003, 8:32–33 ("The pitch of unit cells as shown in FIG. 1 is about 25 μm."). *Grant* explains the well-known concept of pitch, stating that "VDMOS FET gates may be laid out as linear arrays, interdigitated with the source, as shown in Figure 3.9*a* . . . where *a* is the pitch of the array." EX1009, 455. An excerpt of *Grant*'s Figure 3.9*a* is reproduced below, illustrating the pitch

a. Grant illustrates other well-known arrays of unit cells laid out at a regular pitch that have similar cross sections as shown in Figure 3.9a. *See id.* at 70–73, Figure 3.9; *see also id.* at 16, Figure 1.13. EX1002, ¶35.



EX1009, Figure 3.9*a* (excerpted and annotated)

D. Silicon Carbide (SiC)

Historically, power MOSFETs were typically fabricated using monocrystalline silicon (*i.e.*, a single-crystal silicon). But by the early 1990s, an alternative material—silicon carbide—was also known to be particularly well suited for use in such devices. EX1004, 4:22–27 ("Almost all power MOSFETs being marketed today are fabricated in monocrystalline silicon . . . [,] as is known to those skilled in the art, crystalline ***silicon carbide is particularly well suited*** for use in semiconductor devices, and in particular, for power semiconductor devices.)"[1] Silicon carbide was known to have many benefits, including "a wide bandgap, a high melting point, a low dielectric constant, a high breakdown field strength, a high

[1] Unless otherwise noted, all emphasis has been added.

thermal conductivity and a high saturated electron drift velocity compared to silicon." *Id.*, 4:27–31. "These characteristics would allow silicon carbide power devices to operate at higher temperatures, higher power levels and with lower specific on resistance than conventional silicon based power devices." *Id.*, 4:31–34; *see also* U.S. Patent No. 5,510,281 ("*Ghezzo*") (EX1010), 1:52–56 ("Because SiC has a higher critical electric field than silicon, the specific on-resistance of a SiC DMOS is expected to be significantly lower than that of a silicon DMOS with the same high voltage rating."). EX1002, ¶36.

Moreover, *Baliga* teaches that "power MOSFET such as the above described DMOSFET . . . can be readily translated into silicon carbide using known manufacturing techniques." EX1004, 4:35–38. *Baliga* goes on to explain how to translate the DMOSFET into a silicon carbide device using known manufacturing techniques, *e.g.*, by using higher temperature, and longer, diffusions to compensate for the lower diffusion coefficient in silicon carbide. *Id.*, 4:38–43. *Ghezzo*, which issued in 1996 over a decade before the '112 patent was filed, also teaches that "[a] method of implementing vertical power SiC transistor is to replace the conventional double-diffusion with an edge-shifted double ion implantation sequence to overcome the problem of very small dopant diffusivity in SiC" and that "[t]he channel is formed by successive ion implantation of an acceptor atom (such as boron or aluminum) and a donor atom (such as nitrogen or phosphorous) to form the base

and source regions, respectively." EX1010, 1:56–63. Accordingly, SiC power MOSFETs are often referred to as "double-implanted" MOSFETs. *Ghezzo* explains that "[t]he implantations precede the gate electrode formation" because "[t]he self-alignment procedure used for conventional silicon devices cannot be used for SiC because known metal-oxide-semiconductor structures fail to withstand the high temperature of implant activation of about 1500° C." *Id.*, 2:2–12. In other words, implants are activated to form source and drain regions when the surface of the wafer is bare. *See, e.g.*, EX1003, 10:20–25, Figures 3(a) and 3(b). EX1002, ¶37.

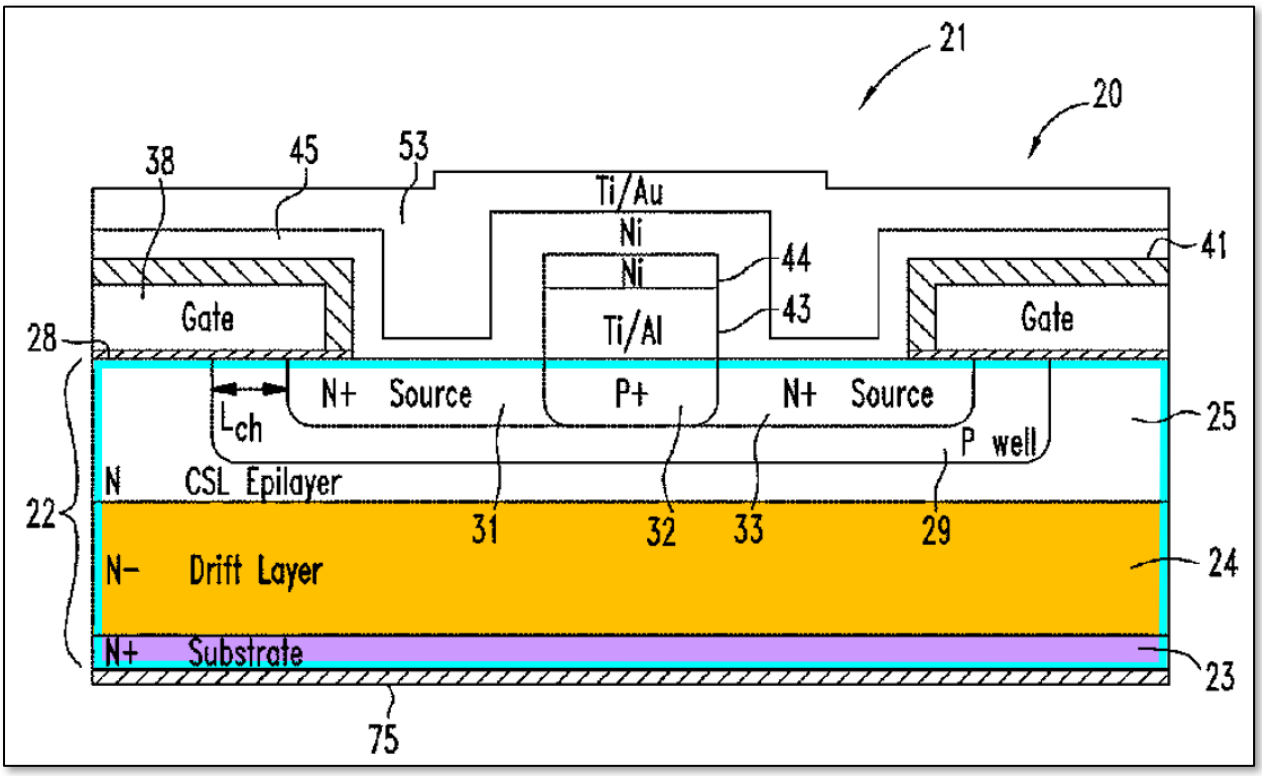
Vertical power MOSFETs made with silicon carbide were well-known long before the '112 patent. EX1002, ¶38.

VII. OVERVIEW OF THE '112 PATENT

A. Alleged Invention

The '112 patent is generally directed to "high voltage power MOSFETs." EX1001, 2:24–26. In particular, the '112 patent describes a vertical MOSFET, having a well-known structure as depicted in Figure 3, which is reproduced below. *Id.*, 1:44; 2:49–50, 3:60–63, Figure 3. Specifically, the MOSFET 21 of Figure 3 includes a silicon-carbide (SiC) **wafer having a substrate body 22** (outlined in cyan below). *Id.*, 4:8–15, 9:26. The **substrate body 22** includes a **substrate 23** (annotated in lavender) and a **drift layer 24** (annotated in orange) formed atop **substrate 23**. *Id.*, 4:8–11. **Substrate 23** is heavily doped with N-type impurities to

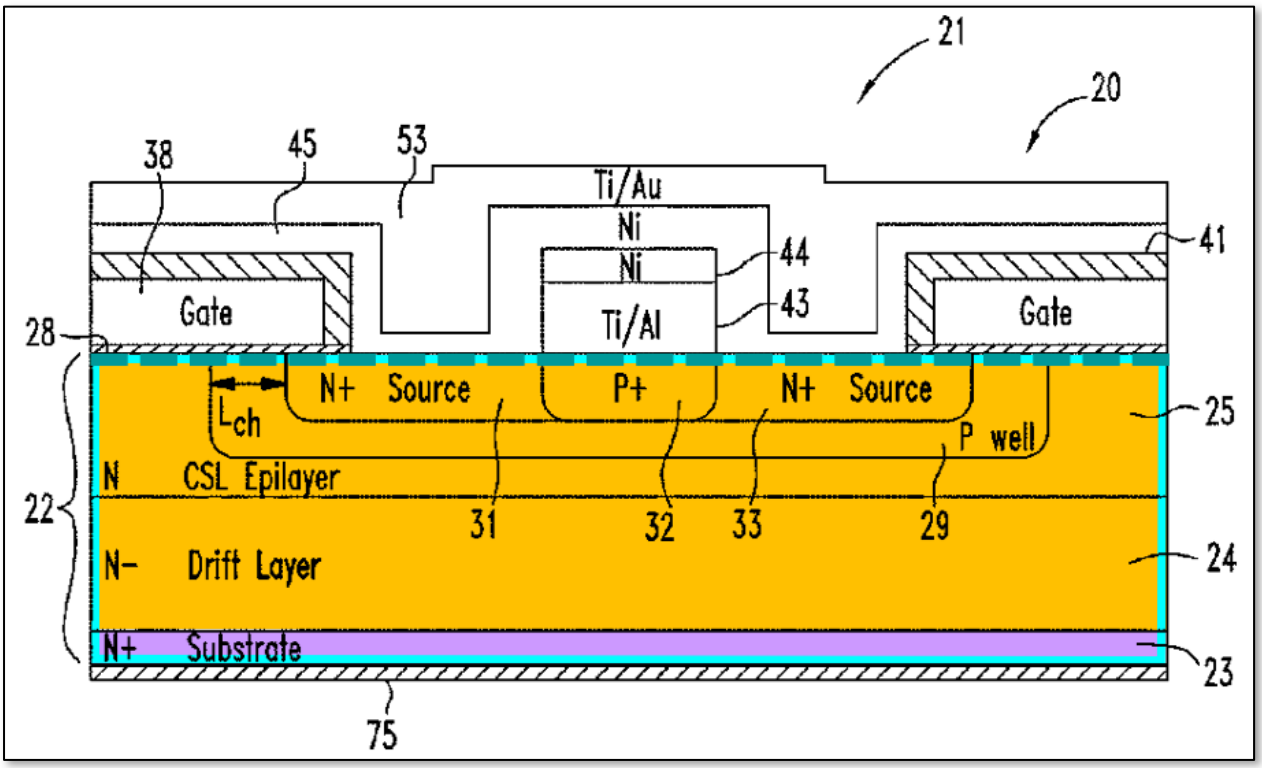
an "N+" concentration, whereas **drift layer 24** is lightly doped to an "N–" concentration. *Id.*, 4:22–25. EX1002, ¶39.



EX1001, FIG. 3 (annotated)

Although the '112 patent illustrates the MOSFET 21 in Figure 3 with a current spreading layer (CSL) 25 formed atop **drift layer 24**, the '112 patent describes an alternative embodiment, "wherein there is no separately formed CSL layer [25], and the **drift layer 24** extends all the way to the top SiC surface 28." *Id.*, 4:25–26, 4:28–30. This embodiment without CSL layer 25 is illustrated below with the CSL 25 in Figure 3 annotated in the same color as **drift layer 24**, such that the **drift layer 24** extends to the **top surface 28**, which is identified with a dashed teal line. Because

the challenged claims 1, 6, 7, and 10–12 do not require a CSL layer, the remainder of this Petition will focus on this alternative embodiment. EX1002, ¶40.

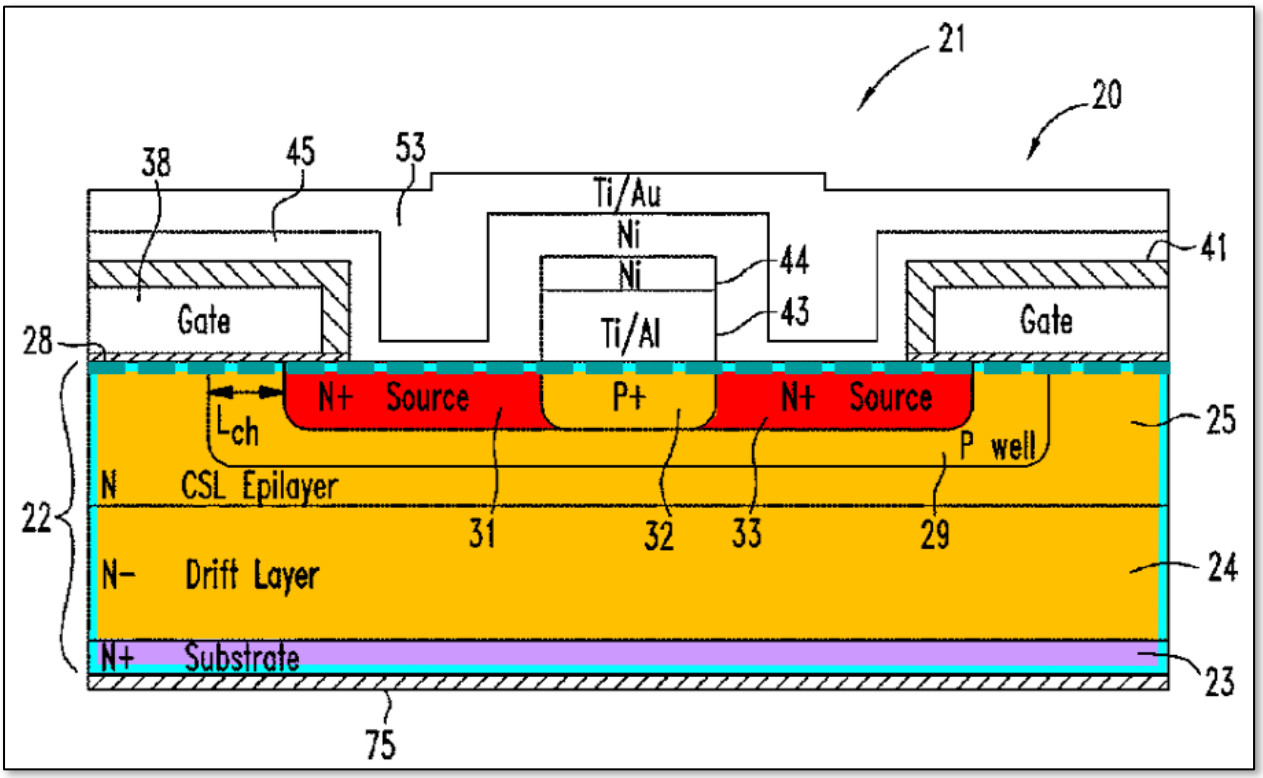


EX1001, FIG. 3 (annotated)

The '112 patent's MOSFET 21 can include a number of implants such as the pair of "heavily doped N+ implant **source regions 31 and 32**"[2] (annotated in red below) located "on opposing sides of a heavily doped, central implant P+ base 33." *Id.*, 4:8–11, 4:51–53. The **source regions 31 and 32** are formed adjacent to the **top**

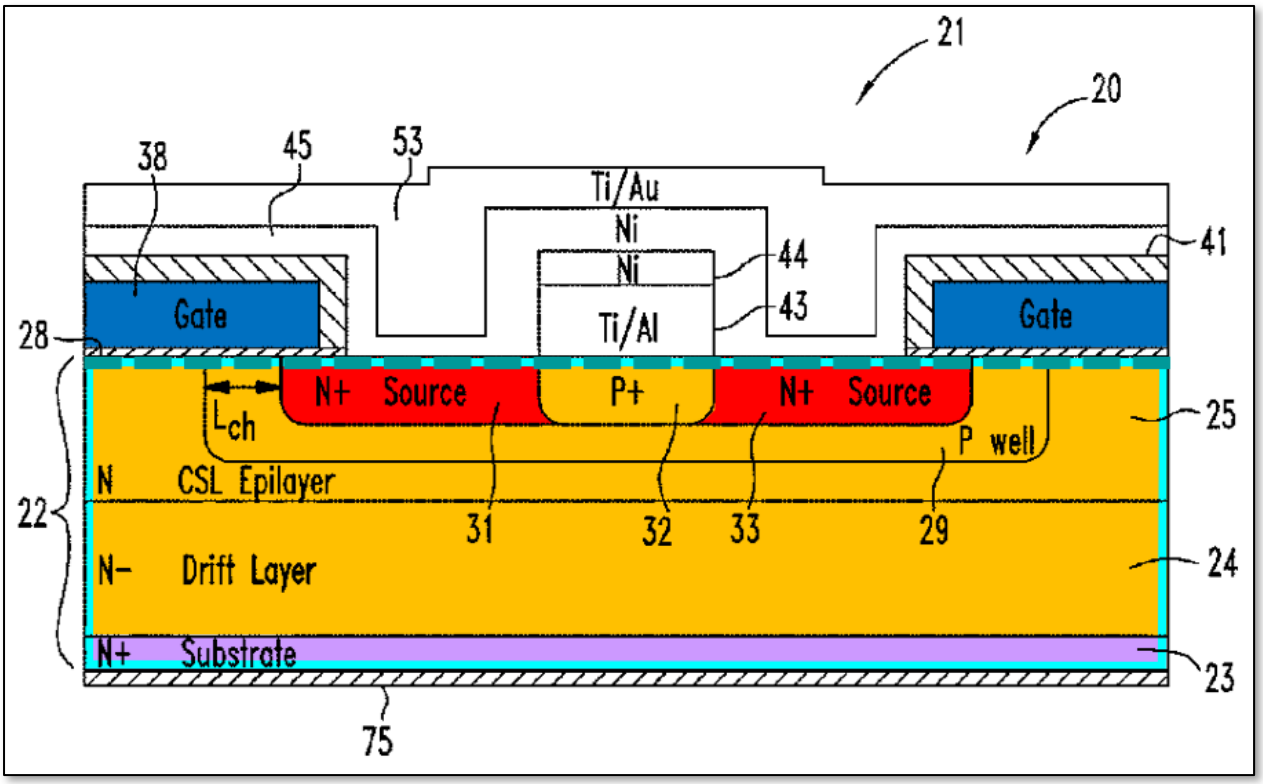
[2] Reference numerals 32 and 33 are interchanged in Figure 3.

surface 28 of the **substrate body 22**. *E.g.*, *id.*, 4:9–11; 8:25–27, 9:27–28. EX1002, ¶41.



EX1001, FIG. 3 (annotated)

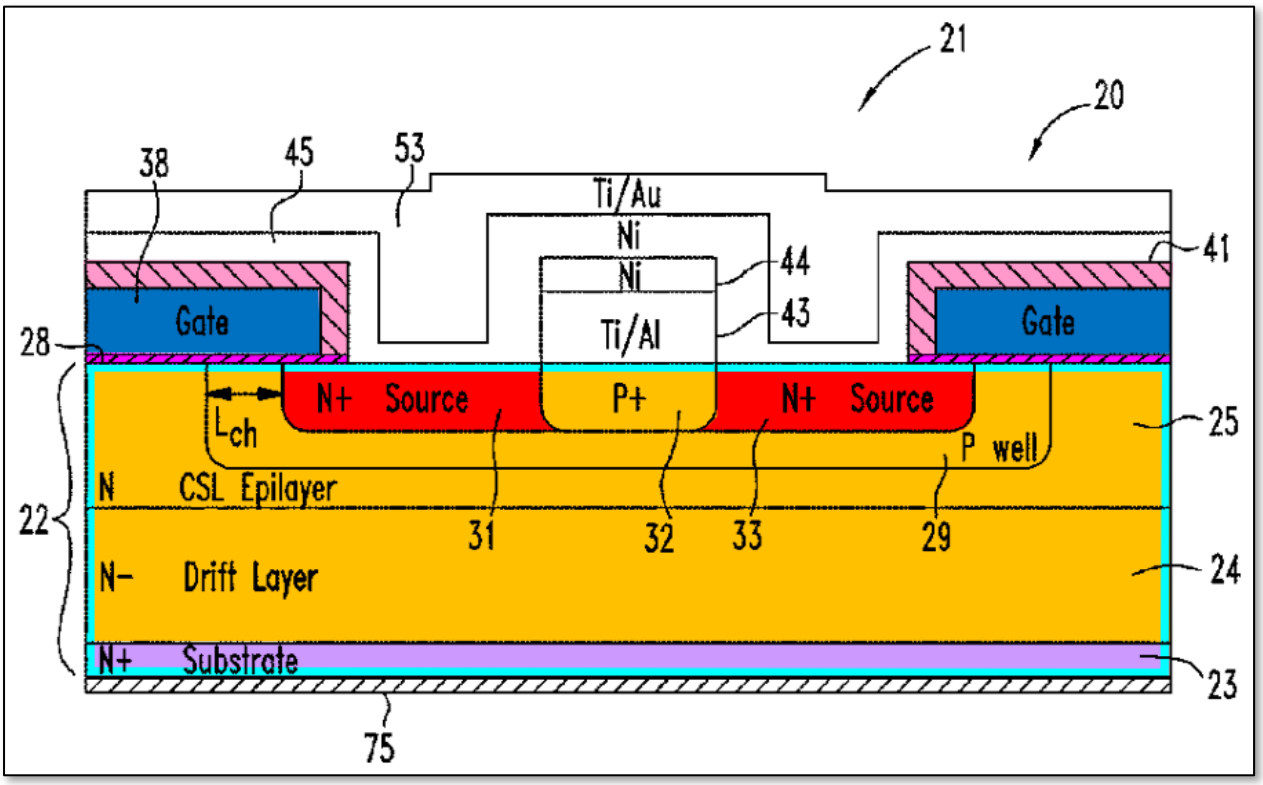
Formed atop the **upper surface 28** are polycrystalline silicon (*i.e.*, polysilicon) **gates 38** (annotated in blue below). *Id.*, 4:66–5:2. EX1002, ¶42.



EX1001, FIG. 3 (annotated)

Each **gate 38** is "surrounded along its top, bottom, left and right sides by an insulating layer of silicon dioxide 41," which the '112 patent also refers to as the "oxide layer 41." *Id.*, 5:2–10. Notably, Figure 3 illustrates and the '112 patent's claims describe that the **oxide layer over the top and sides** (annotated in pink below) of each **gate 38** is ***thicker*** than the **oxide layer beneath** (annotated in magenta) the **gate 38**. *E.g., id.*, 8:33–36, 9:37–39, Figure 3. According to the '112 patent, "[b]ecause it is much thicker, the oxide over the polysilicon gate is not completely removed" during a later etching step in the fabrication process, thus

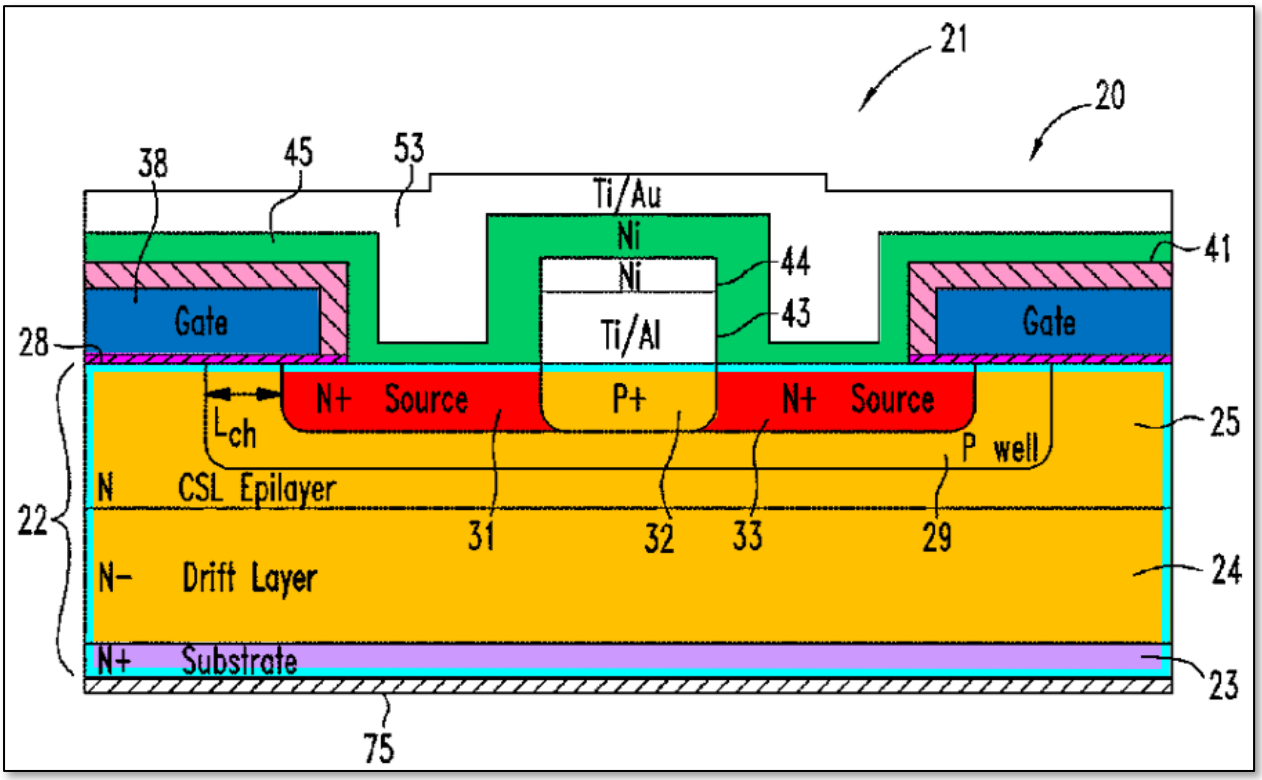
leaving behind "an insulating layer over and around the polysilicon gate." *Id.*, 6:1–4. EX1002, ¶43.



EX1001, FIG. 3 (annotated)

An ohmic **contact metal 45** (annotated in green) is then "formed over the entire MOSFET 21, overlapping the polysilicon **gate 38**, but insulated from it by the thick **oxide 41 on the top and sides** thereof." *Id.*, 5:5–8. According to the '112 patent, "[b]ecause **gate 38** is completely surrounded by insulating **oxide layer 41**, its positionment relative to **source contacts 31 and 32** is much less critical, and it cannot detrimentally come in contact with any portion of the Ni **metal contact 45** due to any mask misalignment during processing." *Id.*, 5:9–13. Further, the '112

patent explains that "the deposition of Ni **metal contact 45** over the entire MOSFET 21 … makes conformal, direct and self-aligning contact … most importantly, with N-**source implants 31 and 32**." *Id.*, 5:19–25. Although the '112 patent describes forming a Ti/Al contact metal 43, and a Ni contact metal 44 atop the P+ base 33 (*see* center of Figure 3 below), none of these features are claimed by the '112 patent. EX1002, ¶44.



EX1001, FIG. 3 (annotated)

As the grounds below demonstrate, the semiconductor structure described and recited in the challenged claims of the '112 patent was well-known in the art before the '112 patent's priority date. EX1002, ¶45.

B. Prosecution History

The '112 patent issued from U.S. Patent Application No. 12/429,176, which was filed on April 23, 2009, claiming priority to U.S. Provisional Application No. 61/047,274 (filed on April 23, 2008).

After a Response to Election/Restriction Requirement and via a Preliminary Amendment, Applicant cancelled original claims 1 and 3 and added new claims 4–18.[3] EX1005, 7–10. The Examiner issued the only Office Action on February 23, 2011, rejecting independent claim 2—among other claims—over prior art references Kumar and Miura and indicating the allowability of independent claim 8. EX1006, 5, 7. The Examiner found claim 8 allowable because the prior art of record "does not teach or suggest the claimed invention having a substrate surface oxidation layer on the upper surface of the substrate body and at least two gates above the substrate surface oxidation layer and a gate oxide layer, thicker than the substrate surface oxidation layer over the tops and sides of each of the gates." *Id.* at 7. In response to the Office Action, with respect to independent claim 2, Applicant argued that the Examiner failed to make out a *prima facie* case of obviousness and that, "[i]n Fig. 1 of Miura the inter-layer insulation film 7 is depicted as being thicker than the gate

[3] Pending independent claims 2 and 8 correspond to issued claims 1 and 6, respectively.

oxide films 5a, but Miura nowhere teaches that either of the gate oxide films 5a/5b are to be thicker or thinner than the inter-layer insulation film 7 or that the drawings are intended to be to scale." EX1007, 12–13. Relatedly, with respect to independent claim 4, Applicant argued that Miura allegedly "discloses only an inter-layer insulation film 7, and nowhere teaches or suggests the composition of such film 7." *Id.* at 11. Therefore, according to Applicant, "Miura does not disclose the composition of the gates or the insulation film, nor does Miura provide any teaching or suggestion what either the gates or insulation film should be made of or what factors would guide such decisions." *Id.*

Applicant went on to assert that "applicant's invention provides for a SiC substrate and polysilicon gates because ***growth*** of the oxidation layer on the polysilicon gates occurs considerably faster than on the SiC substrate." *Id.* at 12. The Examiner subsequently issued a Notice of Allowance on June 29, 2011, without providing any reason for allowing claim 2. EX1008.

As this Petition demonstrates, *Ueno* discloses the allegedly inventive features of the '112 patent, including polysilicon gates and oxide layers formed by the same processes, the "second, thicker oxide layer" recited by claim 1, and the thicker "gate oxide layer" recited by claim 6. EX1002, ¶49.

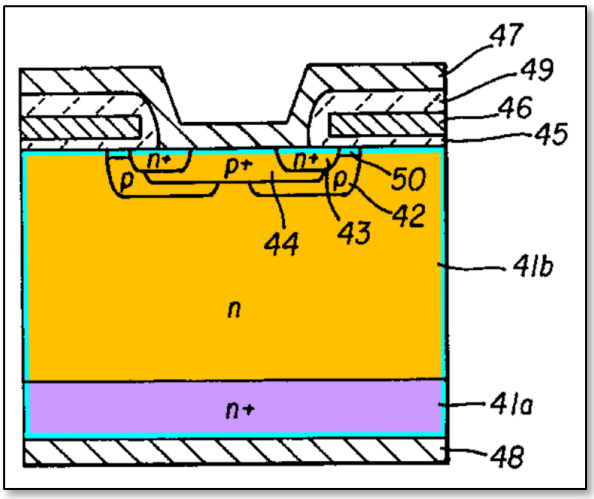
VIII. PRIOR ART PATENTS AND PUBLICATIONS

The following references are pertinent to the grounds of unpatentability:

A. *Ueno*

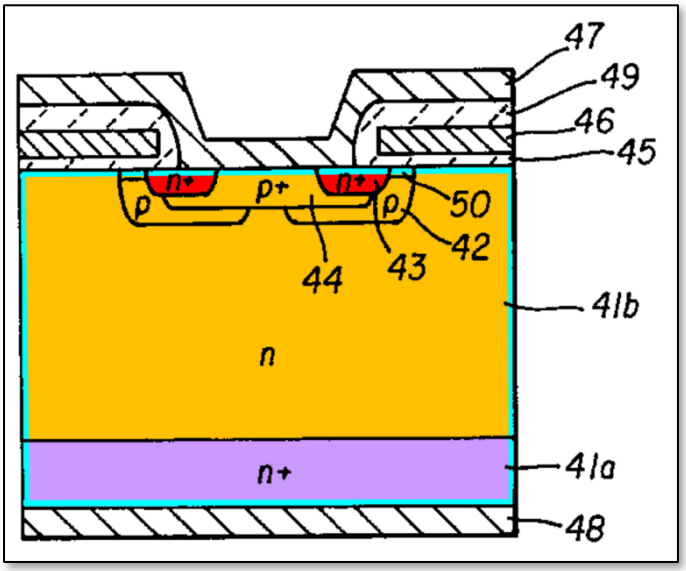
U.S. Patent No. 6,238,980 ("*Ueno*") (EX1003) issued on May 29, 2001. *Ueno* is prior art at least under 35 U.S.C. § 102(b). *Ueno* was of record in the '112 patent's prosecution history, but the Examiner did not describe or address *Ueno* or apply *Ueno* substantively in rejecting the claims.

Like the '112 patent, *Ueno* relates to SiC vertical power MOSFETs. EX1003, 1:7–14, 4:44–50. *Ueno*'s Figure 1 (reproduced below) shows a cross-sectional view of a unit cell of an embodiment of *Ueno*'s SiC vertical MOSFET, which, as explained below, is strikingly similar to the '112 patent's MOSFET 21. EX1003, 7:31–33, 7:65–67; EX1001, Figure 3. In Figure 1, *Ueno* discloses a **wafer** (outlined in cyan below) in which an n **drift layer 41b** (annotated in orange) is grown on an "n+ drain layer or **substrate 41a**" (annotated in lavender). EX1003, 8:1–13, 8:54–55. EX1002, ¶51.



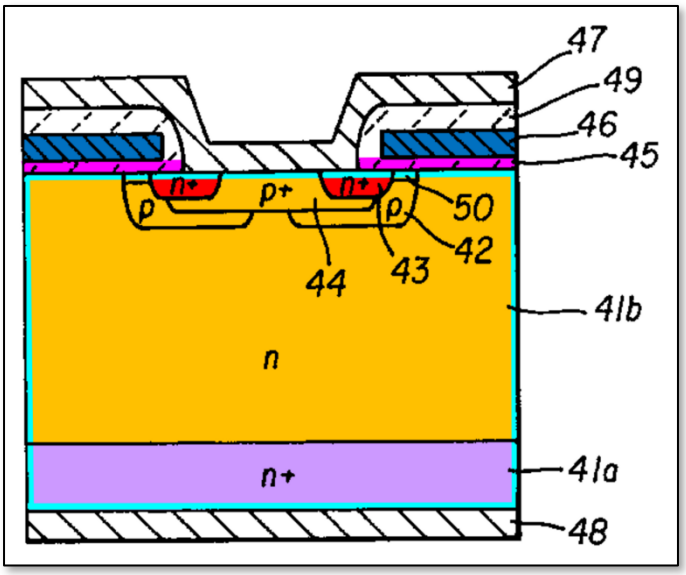
EX1003, FIG. 1 (annotated)

Ueno further discloses that "a p base region 42 is formed in a surface layer of the n **drift layer 41b**, and an n+ **source region 43** is formed within the p base region 42." *Id.*, 8:2–4. As shown in Figure 1, the unit cell of *Ueno*'s vertical MOSFET includes two **source regions 43**, which are annotated in red below. EX1002, ¶52.



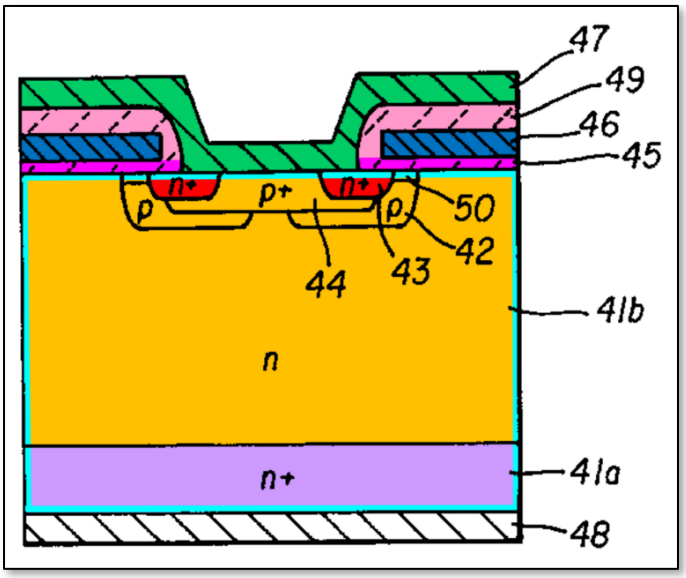
EX1003, FIG. 1 (annotated)

Gates (annotated in blue below) are formed—by patterning a polysilicon film "to provide the gate electrode layer[s] 46"—on **gate oxide film 45** (annotated in magenta) over the surface of the n **drift layer 41b**. *Id.*, 8:6–10, 10:42–44, Figures 3c and 3d. EX1002, ¶53.



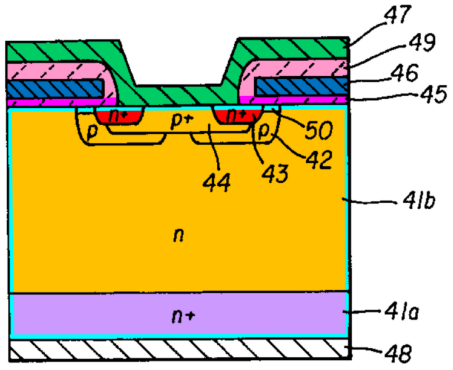
EX1003, FIG. 1 (annotated)

A **source electrode 47** (annotated in green below) is formed to be in contact with the n+ **source regions 43**. *Id.*, 8:10–11. An **interlayer insulating film 49** (annotated in pink below), in the form of a silicon oxide film, insulates each **gate** from the **source electrode 47**. *Id.*, 8:13–16. The **interlayer insulating film 49** is grown by subjecting the **gates** to thermal oxidation. *Id.*, 10:42–47, Figures 3d–3f. *Ueno* discloses that "[t]he thickness of the **gate oxide film [45]** is 50 nm, . . . while the thickness of the **interlayer insulating film 49** is 2 μm." *Id.*, 8:29–32. EX1002, ¶54.

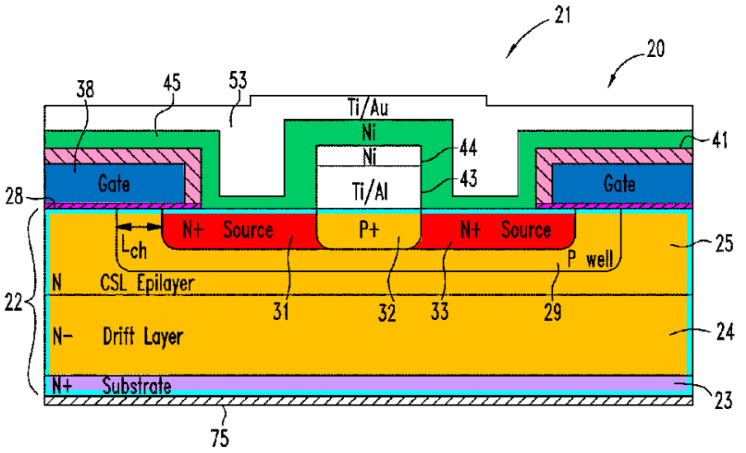


EX1003, FIG. 1 (annotated)

Comparing *Ueno*'s Figure 1 with the '112 patent's Figure 3 reveals that *Ueno* discloses the same relevant semiconductor structure as the '112 patent. In the '112 patent's MOSFET 21, the Ti/Al contact metal 43 and the Ni contact metal 44 are added to the basic structure to purportedly improve the quality of the electrical contact to the P+ base 33, but are not relevant to this Petition because they are not recited in any challenged claim of the '112 patent. EX1002, ¶55.



EX1003, FIG. 1 (annotated)

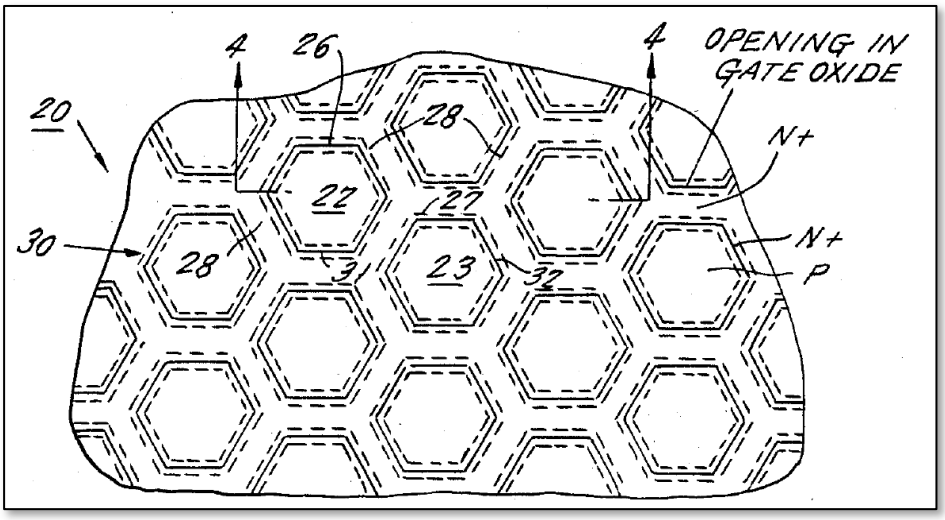


EX1001, FIG. 3 (annotated)

B. *Lidow*

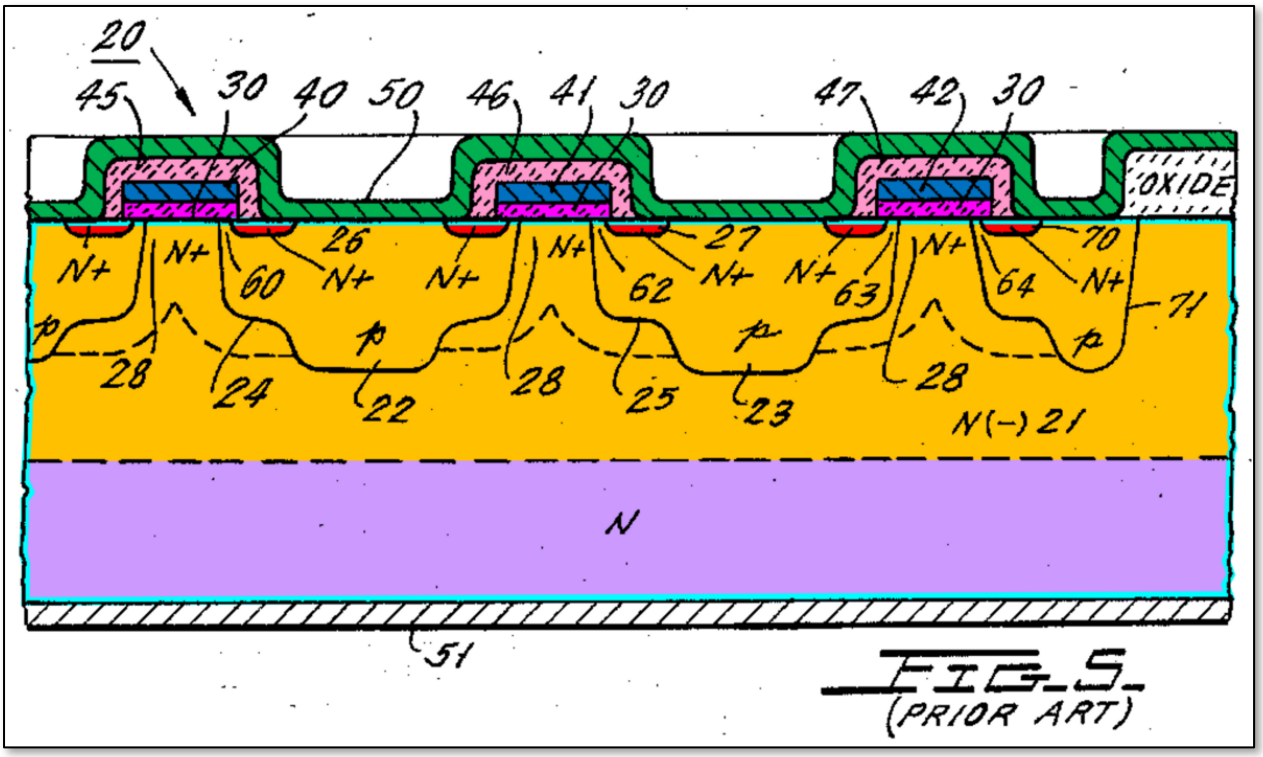
U.S. Patent No. 4,593,302 ("*Lidow*") (EX1014) issued on June 3, 1986, and is prior art at least under 35 U.S.C. § 102(b). *Lidow* was not of record in the '112 patent's prosecution history.

Like the '112 patent and *Ueno*, *Lidow* relates to power MOSFETs. EX1014, 1:22–25, Figures 1–5. In particular, *Lidow* discloses a prior-art high power MOSFET device consisting of a plurality of hexagonal cells. *See id.*, Figures 2–5, 4:44–46, 6:54–55. In Figure 3 (reproduced below), *Lidow* illustrates a plan (*i.e.*, top) view of a small portion of the uniformly spaced hexagonal cells of the MOSFET device. *Id.*, 3:28–30. EX1002, ¶56.



EX1014, FIG. 3

Lidow illustrates a cross-sectional view of the MOSFET device in Figure 5 (reproduced below), taken across the section line 4-4 in Figure. 3. *Id.*, 3:31–35. *Lidow* explains that "the hexagonal source regions are formed in a **semiconductor body or wafer** which is an **N type wafer** 20 of monocrystalline silicon which has a thin **N− epitaxial region 21** deposited thereon." *Id.*, 4:50–53. Below, the **semiconductor body** is outlined in cyan, and the **N type wafer** is annotated in lavender and the **N− epitaxial region 21** in orange. EX1002, ¶57.

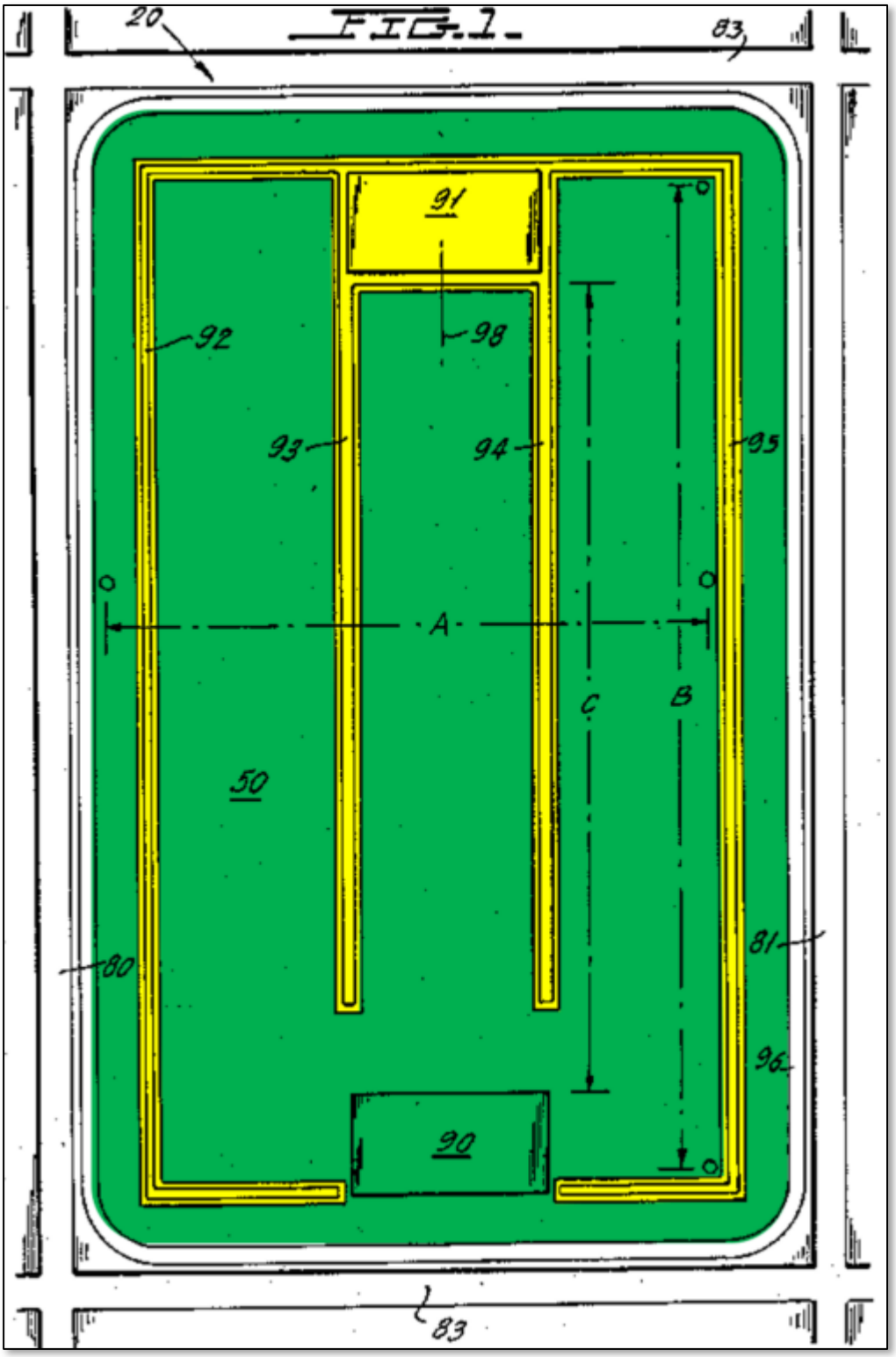


EX1014, FIG. 5 (annotated)

In Figure 5, *Lidow* also illustrates **N+ type source regions 26** (annotated in red above), **polysilicon gates 40, 41, 42** (annotated in blue), **oxide layer 30** (annotated in magenta), **silicon dioxide coating sections 45, 46, 47** (annotated in pink), and **source electrode 50** (annotated in green). *Id.*, 5:13 ("N+ regions 26), 5:30 ("N+ type source rings 50), 5:37 ("polysilicon sections 40, 41 and 42"), 5:57 ("gate 40"), 5:23–26 ("an oxide layer . . . shown as the insulation layer 30"), 5:39–41 ("A silicon dioxide coating is then deposited atop the polysilicon grid 40 shown as coating sections 45, 46 and 47 . . ."), 5:44–46 ("the source electrode is shown as

conductive coating 50 which may be of any desired material, such as aluminum"). EX1002, ¶58.

Notably, the **source electrode 50** is a conductor that extends over and between the **silicon dioxide coating sections 45, 46, 47** and the **polysilicon gates 40, 41, 42** and is in electrical contact with the **N+ type source regions 26**. EX1014, 5:58–59 ("the source region 26, which is connected to the conductor 50"). Furthermore, *Lidow* discloses that the **source electrode 50** is "deposited over the entire upper surface of the wafer." *Id.*, 5:42–44. Indeed, as *Lidow* illustrates in a plan view of the MOSFET device in Figure 1 (reproduced below), the **source electrode 50** (annotated in green below) covers substantially the entire upper surface of the MOSFET device, except for a portion (annotated in yellow) where a "gate connection pad 91 is electrically connected to a plurality of extending fingers 92, 93, 94 and 95 which . . . make electrical connection to the polysilicon gate . . ." *See id.*, 3:21–23, 6:14–19, 6:32–36; *see also id.*, Figure 2; *cf.* EX1001, 7:37–38 ("bonding pad for the polysilicon gate"), Figure 9 (illustrating a "Gate Contact Pad" on top of a MOSFET in a plan view). EX1002, ¶59.



EX1014, FIG. 1 (annotated)

IX. CLAIM CONSTRUCTION

During IPR, claims are construed according to the "*Phillips* standard." *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc); 83 Fed. Reg. 51341 (Oct. 11, 2018). The Board need only construe the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Sys., Inc.*, IPR2015-00633, Paper No. 11 at 16 (Aug. 14, 2015); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Here, given the close correlation between the asserted prior art and the challenged claims of the '112 patent, the Board need not construe any terms of the challenged claims to resolve the underlying controversy, as any reasonable interpretation of those terms consistent with their plain meaning (as would have been understood by a POSITA at the time of the invention, having taken into consideration the language of the claims, the specification, and the prosecution history of record) reads on the prior art.[4]

X. SPECIFIC GROUNDS FOR UNPATENTABILITY

Under 37 C.F.R. § 42.104(b)(4)–(5), the following sections (as confirmed in Dr. Subramanian's declaration, EX1002, ¶¶60–133) detail the grounds of

[4] Petitioner reserves all rights to raise claim construction and other arguments in this and other proceedings as relevant and appropriate.

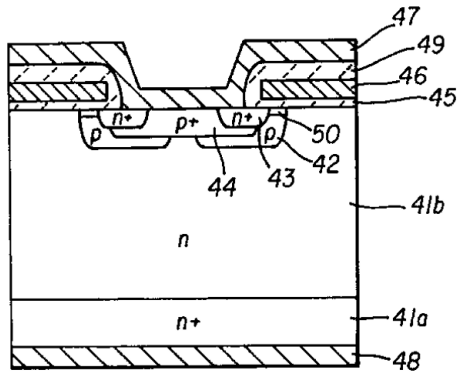
unpatentability, the limitations of challenged claims 1, 6, 7, and 10–12 of the '112 patent, and how these claims were therefore obvious in view of, the prior art. EX1002, ¶¶60–133.

A. Ground I: Claims 1, 6, 7, 10, and 12 are Obvious Over *Ueno*

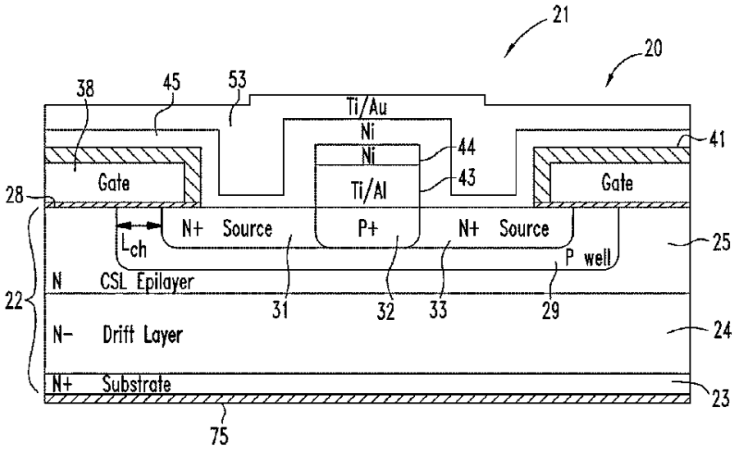
1. Independent Claim 1

a) 1[preamble]: "A silicon carbide power MOSFET, comprising:"

Regardless of whether the preamble is limiting, *Ueno* discloses it. *Ueno* explicitly discloses that "FIG. 1 is a cross-sectional view showing a part of a **SiC** vertical **MOSFET** . . ." EX1003, 7:31–32. "SiC" is a standard term and chemical abbreviation for referring to silicon carbide. *See, e.g.*, EX1011, 658 ("silicon carbide (SiC)"); EX1012, 956 ("Silicon carbide (SiC)"). *Ueno* uses "SiC" in the conventional way to refer to silicon carbide. EX1003, 1:18 ("Silicon carbide (hereinafter referred to as 'SiC')"). *Ueno*'s Figure 1 is reproduced below for comparison with the '112 patent's Figure 3. EX1002, ¶62.



EX1003, FIG. 1



EX1001, FIG. 3

Further, *Ueno* discloses that its invention relates to "a method for manufacturing silicon carbide MOS semiconductor devices, such as MOS field-effect transistors (hereinafter referred to as '**MOSFET**'), having a MOS type gate of metal-oxide-semiconductor structure, which use **silicon carbide** as a semiconductor material and serve as **power** semiconductor devices." EX1003, 1:7–14 (emphasis added). *See also id.*, 3:3–5. Thus, *Ueno*'s MOSFET is "*a silicon carbide power MOSFET*." EX1002, ¶63.

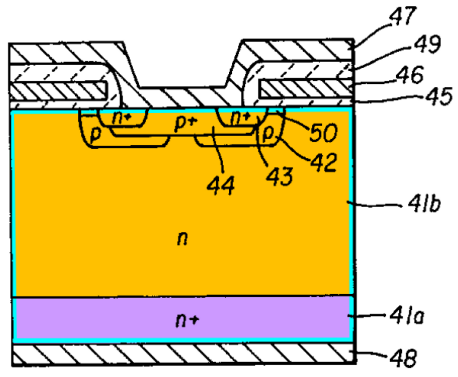
b) 1[a]: "a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof;"

Ueno discloses element 1[a]. As explained below, *Ueno* discloses a **silicon carbide wafer** having an n **drift layer 41b** grown ***on*** **substrate 41a**. Moreover, *Ueno*'s **drift layer 41b** has two (*i.e.*, "*a plurality of*") **source regions 43** formed adjacent its **upper surface**. EX1002, ¶64.

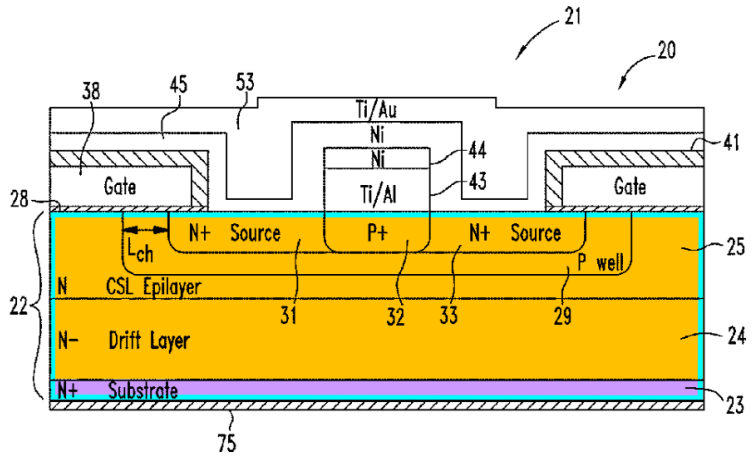
i. 1[a1]: "a silicon carbide wafer having a substrate and a drift layer on said substrate"

Ueno discloses element 1[a1]. *Ueno* explicitly discloses a **wafer** in which an n **drift layer 41b** is grown ***on*** an n+ drain **layer 41a**. EX1003, 8:1–2, 8:54–55. *Ueno* uses "drain layer" and "substrate" interchangeably to refer to layer 41a. *Id.*, 8:12–13 ("n+ drain layer or substrate 41a"). *Ueno* also discloses that "the n **drift layer 41b** doped with phosphorous is epitaxially ***grown on*** the n+ drain **layer 41a**,

to provide a 4H-SiC substrate." *Id.*, 8:54–56. Thus, *Ueno*'s **drift layer 41b** is on **substrate 41a**. 4H-SiC is a type of ***silicon carbide***. *See id.*, 7:61–67. *Ueno's* Figure 1 is reproduced below side-by-side with the '112 patent's Figure 3, with the **wafers** in cyan, **substrates** in lavender, and **drift layers** in orange. EX1002, ¶65.



EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

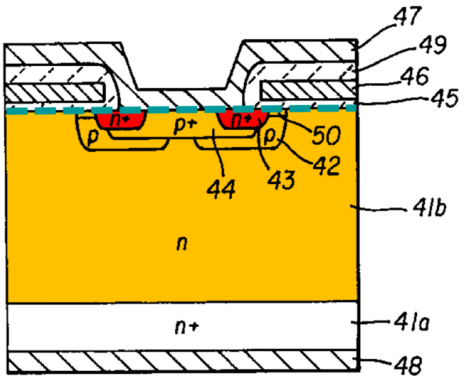
Ueno states that, "[w]hile numerous polytypes of silicon carbide are available, 6H-SiC and 4H-SiC are mainly employed in the following embodiment." EX1003, 7:61–64. A POSITA would have understood this disclosure to mean that both *Ueno*'s **drift layer 41b** and **substrate 41a** are made of silicon carbide. Because *Ueno*'s drift layer and substrate are silicon carbide, it would have been obvious for *Ueno*'s **wafer** to be silicon carbide. In particular, a POSITA would have understood that silicon carbide chips were formed from silicon carbide wafers, *e.g.*, by epitaxially growing layers on the wafer. *See id.*, 5:48–51 ("epitaxially growing a first conductivity type drift layer comprising silicon carbide, on a silicon carbide substrate, to provide a silicon carbide substrate"), 8:54–56 ("the n **drift layer 41b**

doped with phosphorous is epitaxially grown on the n+ drain **layer 41a**, to provide a 4H-SiC substrate"); *see also* EX1021, 284 ("4H- and 6H-SiC wafers"); *id.* ("The controlled growth of high-quality epilayers is naturally a key issue in the realization of SiC electronics."). Indeed, a POSITA would have understood that forming silicon carbide chips, like *Ueno*'s, from silicon carbide wafers was overwhelmingly the most common way of forming such chips. Further, a POSITA would have understood that the most common fabrication technique for silicon carbide chips such as *Ueno*'s would have been to form many such chips simultaneously on a silicon carbide wafer and then saw the wafer into individual chips or dies, just as was commonly done for silicon wafers. *See e.g.,* EX1023, 6 ("Tens or hundreds of identical chips are fabricated simultaneously on a silicon wafer."); *id.,* 5, Figures 1.3 and 1.5. Accordingly, *Ueno* teaches "*a silicon carbide wafer having a substrate and a drift layer on said substrate*." EX1002, ¶66.

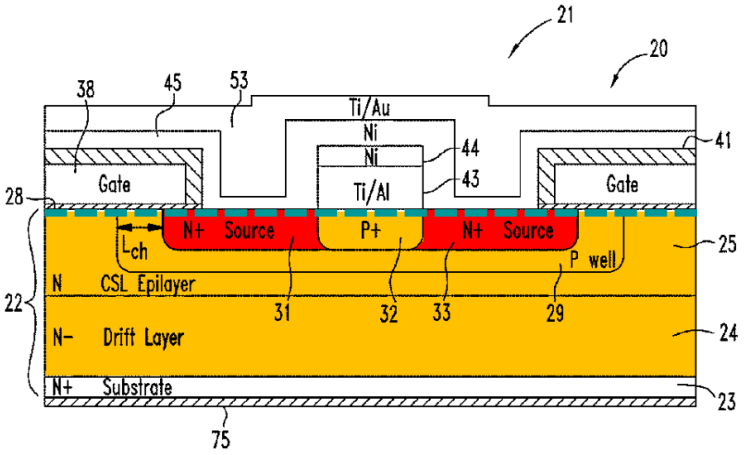
ii. 1[a2]: "said drift layer having a plurality of source regions formed adjacent an upper surface thereof"

Ueno discloses element 1[a2]. *Ueno*'s Figure 1 shows the **drift layer 41b** having two (*i.e.*, "*a plurality of*") **source regions 43** (annotated in red below) formed adjacent an **upper surface** (identified with a dashed teal line, below) of the **drift layer 41b**. EX1003, 8:11 ("source region 43"). A side-by-side comparison below

with the '112 patent's Figure 3 shows that, in both *Ueno* and the '112 patent, the **source regions** are below and adjacent the **upper surface**. EX1002, ¶67.

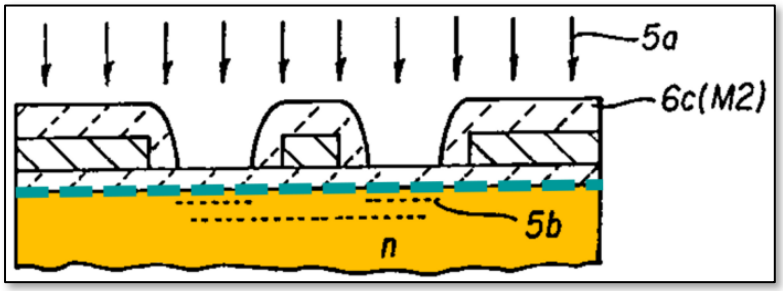


EX1003, FIG. 1 (annotated)



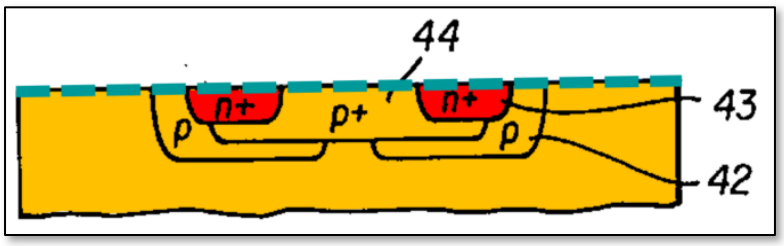
EX1001, FIG. 3 (annotated)

Ueno also discloses the formation of the sources adjacent the upper surface. Specifically, with regard to the process steps for manufacturing the MOSFET of Figure 1, *Ueno* discloses that "nitrogen (N) ions 5a for forming the n+ **source region 43** are implanted" and notes that, in Figure 2g (reproduced below), "reference numeral 5b denotes nitrogen atmos [*sic*] thus implanted." EX1003, 9:59–62, Figure 2g. As can be seen in Figure 2g, the nitrogen atoms 5b are adjacent the **upper surface** of the **drift layer 41b**. EX1002, ¶68.



EX1003, FIG. 2g (annotated)

Furthermore, *Ueno* discloses that, after a heat treatment to activate implanted impurities, the **source regions 43** are formed as *Ueno* illustrates in Figure 3b (reproduced below). *Id.*, 10:19–24. Indeed, the **source regions 43** are formed adjacent the **upper surface** of the **drift layer 41b**. EX1002, ¶69.



EX1003, FIG. 3b (annotated)

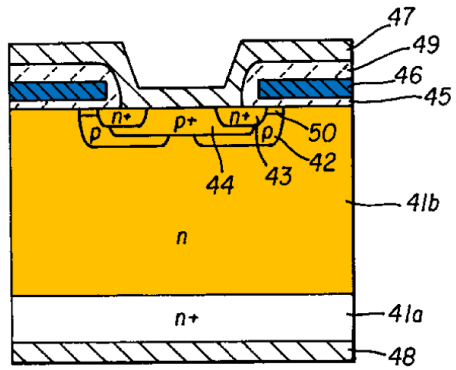
Accordingly, *Ueno* discloses "*said drift layer having a plurality of source regions formed adjacent an upper surface thereof*." EX1002, ¶70.

c) 1[b]: "a plurality of polysilicon gates above said drift layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions, said first gate having a top surface, a lower surface and a sidewall, said sidewall overlying said first source region;"

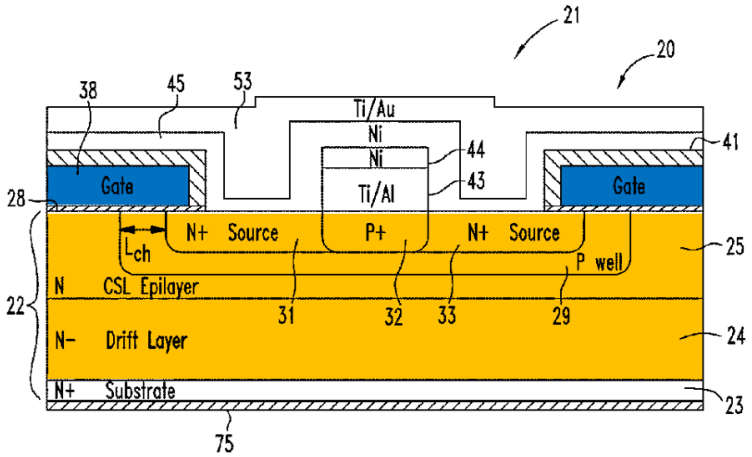
Ueno renders obvious element 1[b]. As explained below, *Ueno* explicitly discloses two (*i.e.*, "*a plurality of*") **gates** above the **drift layer 41b**. EX1003, 8:6–9 ("drift layer 41b"), Figure 1. Moreover, each of the two polysilicon **gates** is adjacent a corresponding one of the two **source regions 43**. As shown in more detail below, *Ueno*'s Figure 1 illustrates that the right **gate** (*i.e.*, "*said first gate*") has a **top surface**, a **lower surface**, and a **sidewall** that overlies the right **source region 43** (*i.e.*, "*said first source region*"). EX1002, ¶71.

i. 1[b1]: "a plurality of polysilicon gates above said drift layer"

Ueno discloses element 1[b1]. *Ueno*'s Figure 1 shows two (*i.e.*, "*a plurality of*") **gates** above the **drift layer 41b**. EX1003, 8:6 ("gate electrode layer 46"), 8:8–9 ("drift layer 41b"), Figure 1. *Ueno* discloses that "***polysilicon*** film 1c is patterned by photolithography, to provide the gate electrode layer 46." *Id.*, 10:42–44, Figures 3c and 3d. The patterning of polysilicon film 1c into individual structures 46, as *Ueno* shows in Figure 3d, forms polysilicon **gates**. A side-by-side comparison below with the '112 patent's Figure 3 shows that, in both *Ueno* and the '112 patent, the **gates** are above the **drift layer**. EX1002, ¶72.



EX1003, FIG. 1 (annotated)

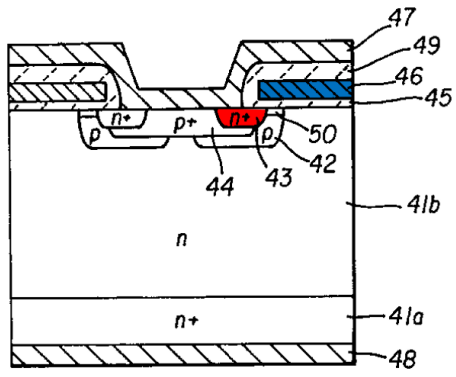


EX1001, FIG. 3 (annotated)

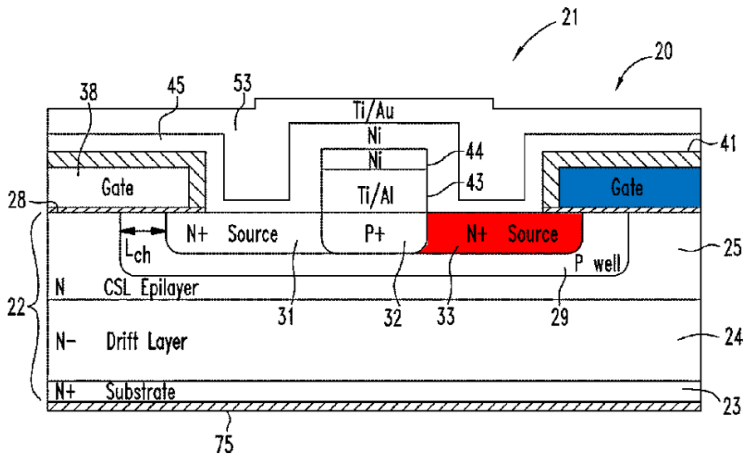
Accordingly, *Ueno* discloses "*a plurality of polysilicon gates above said drift layer*." EX1002, ¶73.

ii. 1[b2]: "said plurality of polysilicon gates including a first gate adjacent a first of said source regions"

Ueno discloses element 1[b2]. Each of the two **gates** that *Ueno* illustrates in Figure 1 is adjacent a corresponding one of the two **source regions 43**. For example, the **gate** on the right (*i.e.*, "*a first gate*"), is adjacent the right **source region 43** (*i.e.*, "*a first of said source regions*"). Just as in the '112 patent, *Ueno*'s **gates** and **source regions 43** are adjacent one another and separated by a thin gate oxide layer. In both *Ueno* and the '112 patent, the **gates** include a first **gate** adjacent a first **source region**, as shown by the side-by-side comparison below with the '112 patent's Figure 3. EX1002, ¶74.



EX1003, FIG. 1 (annotated)



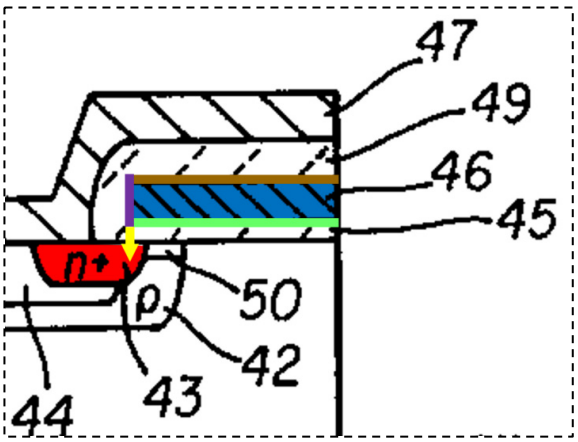
EX1001, FIG. 3 (annotated)

iii. 1[b3]: "said first gate having a top surface, a lower surface and a sidewall, said sidewall overlying said first source region"

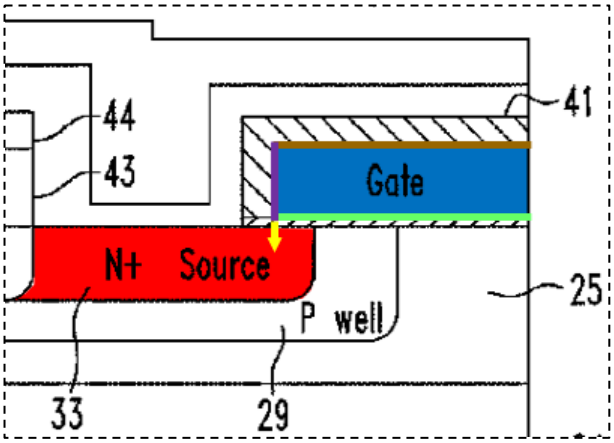
Ueno renders obvious element 1[b3]. As illustrated in the excerpt of *Ueno*'s Figure 1 below, the right **gate** (*i.e.*, "*said first gate*") has a **top surface** (outlined in

brown), a **lower surface** (outlined in lime), and a **sidewall** (outlined in purple). As further illustrated by the yellow arrow, the **sidewall** overlies the right **source region 43** (*i.e.*, "*said first source region*"). In both *Ueno* and the '112 patent, each of the **gates** has a **top surface**, a **lower surface**, and a **sidewall**, and the **sidewall** overlies a **source region**, as shown below by the side-by-side comparison with the '112 patent's Figure 3. Moreover, a POSITA would have found it obvious to do so. In both *Ueno* and the '112 patent, the gate is created after the base and source regions, and the gate location is defined with a separate masking step. *Compare* EX1001, 5:51–60, Figures 5 and 6 *with* EX1003, 10:20–44, Figures 3(b)–(d); *see also* EX1010, 2:2–3 ("The implantations precede the gate electrode formation."). As a result, both *Ueno*'s manufacturing process and the disclosed process in the '112 patent align the gate to the previously formed source region so as to fully cover the channel region—*i.e.*, the portion of the p-well that is under the gate. It was well known in the art to provide alignment tolerance by adding gate-source overlap, to account for the imperfect alignment that is possible in real manufacturing processes. A POSITA would have appreciated the desirability of having an alignment tolerance to account for the lack of self-alignment between the source region and the gate. Such an alignment tolerance was well-known and was used in the pre-polysilicon gate era when metal gates had to be formed after source regions in silicon MOSFETs. *See, e.g.*, EX1022, 504–505 ("In the metal-gate process . . . [t]o ensure that the source

and drain are bridged by the gate, ***overlap*** for alignment tolerance must be allowed."). Figure 1 of *Ueno* depicts this overlap, but *Ueno* does not provide a textual description of the overlap. However, because of the standard practice of providing an overlap for alignment tolerance, even without textual description of the gate overlying the source by *Ueno*, it would have been obvious for the gate to have a sidewall overlying the source. Further, a POSITA would have recognized the overlap shown in *Ueno*'s Figure 1 to be intentional. Indeed, the background prior art discussed *supra* all also show such an overlap and a POSITA would have found it obvious to use one. *See* EX1009, Figure 3.9*a*; EX1004, Figure 1; EX1014, Figure 5. EX1002, ¶75.



EX1003, FIG. 1
(excerpted and annotated)

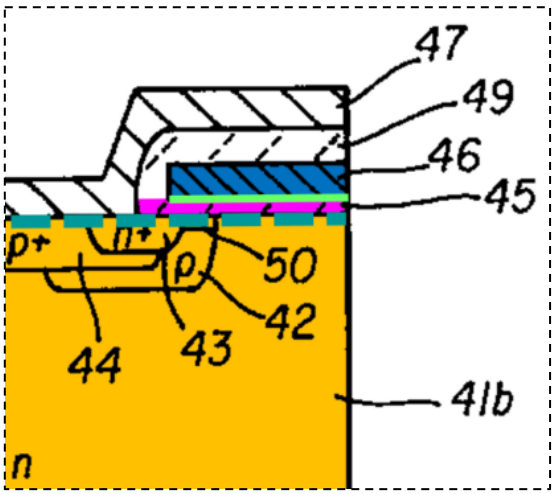


EX1001, FIG. 3
(excerpted and annotated)

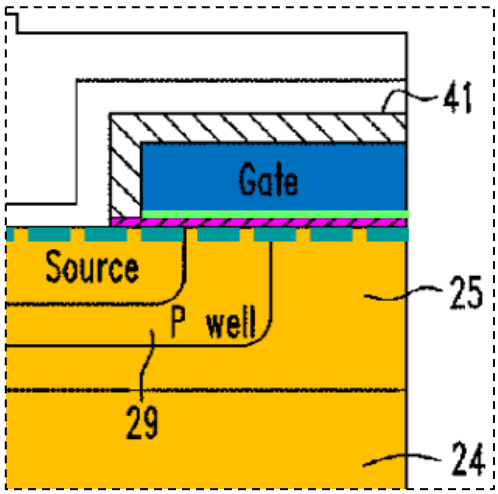
d) 1[c]: "a first oxide layer between said first gate lower surface and said upper surface of said drift layer;"

Ueno discloses element 1[c]. *Ueno*'s Figure 1 shows a **gate oxide film 45** (annotated in magenta below) (*i.e.*, "*a first oxide layer*") between the **lower surface**

of the right **gate** (*i.e.*, "*said first gate*") and the **upper surface** (identified with a dashed teal line, below) of the **drift layer 41b**. EX1003, 8:7 ("gate oxide film 45"). A side-by-side comparison below with the '112 patent's Figure 3 shows that, in both *Ueno* and the '112 patent, there is a **gate oxide** between the **lower surface** of the **gate** and the **upper surface** of the **drift layer 41b**. *See id.*, 8:6–10. EX1002, ¶76.



EX1003, FIG. 1
(excerpted and annotated)



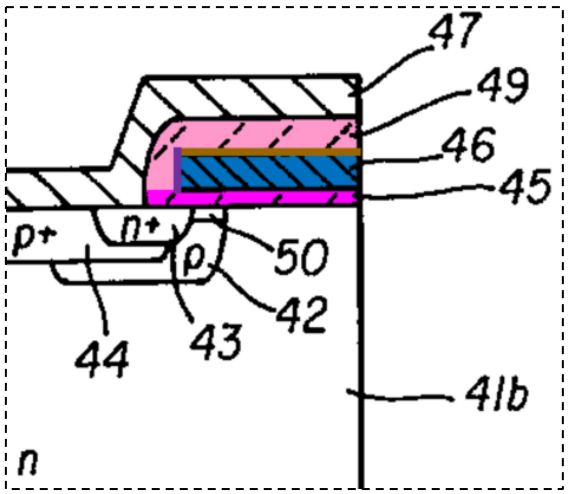
EX1001, FIG. 3
(excerpted and annotated)

As *Ueno* explains when describing the process steps for manufacturing the MOSFET of Figure 1, "an oxide film 6d that . . . provides the **gate oxide film 45** is formed," followed by the deposition of the polysilicon film 1c that provides the **gates**. EX1003, 7:37–39, 10:35–40, Figure 3c. As *Ueno* shows in Figures 3c and 3d, the oxide film 6d is formed on the upper surface of the **drift layer 41b** and is covered by the polysilicon film 1c, which is subsequently patterned to form the **gates**. *Id.*, Figures 3c and 3d. Thus, the **gate oxide film 45** is between the **lower**

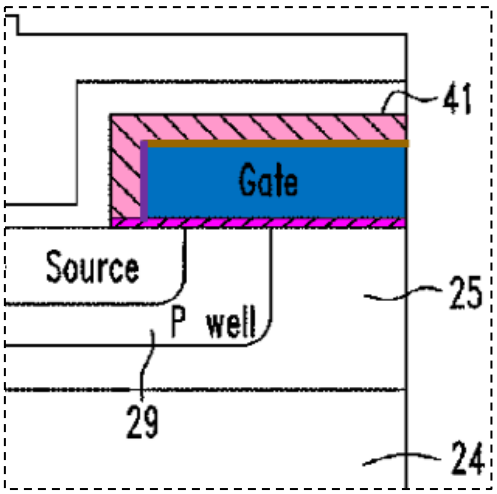
surface of the right gate and the upper surface of the drift layer 41b. EX1002, ¶77.

e) 1[d]: "a second, thicker oxide layer over said top surface and sidewall of said first gate; and"

Ueno discloses element 1[d]. In one of the process steps for manufacturing the MOSFET of Figure 1, *Ueno* discloses that, after "the oxide film 6e is subjected to wet etching or dry etching," "[t]he oxide film 6e formed ***on and along the side*** of the gate electrode layer 46 provides the interlayer insulating film 49" (annotated in pink below). EX1003, 7:37–39, 10:48–61, Figures 3e and 3f. *Ueno*'s excerpted Figure 1 below illustrates the interlayer insulating film 49 ("*a second oxide layer*") over the top surface (outlined in brown) and the sidewall (outlined in purple) of the right gate (*i.e.*, "*said first gate*"). A comparison below between *Ueno*'s Figure 1 and the '112 patent's Figure 3 shows that, in both *Ueno* and the '112 patent, there is a thick oxide layer on the top surface and sidewall of the gate. EX1002, ¶78.



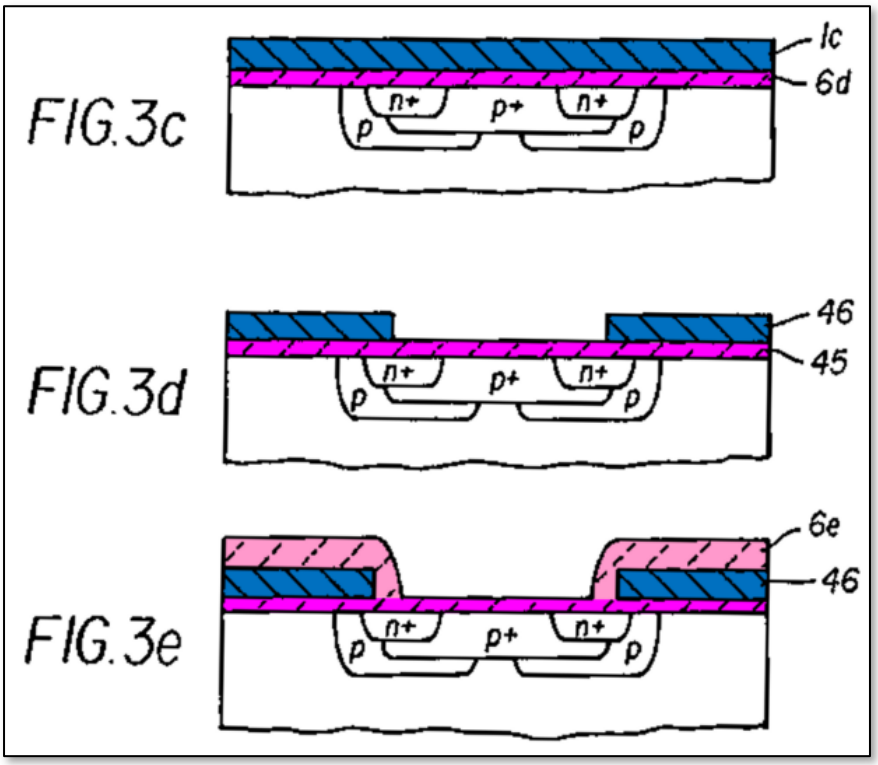
EX1003, FIG. 1



EX1001, FIG. 3

(excerpted and annotated) | (excerpted and annotated)

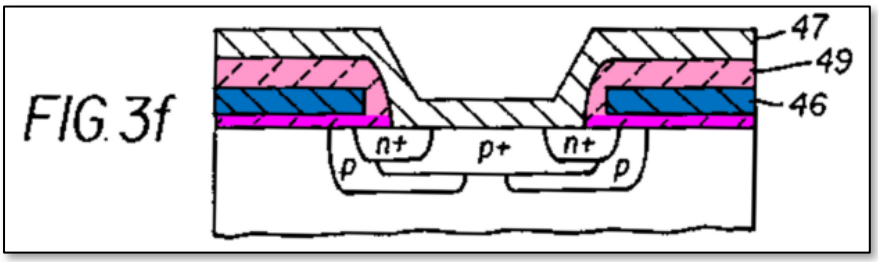
Moreover, *Ueno* describes that, after the polysilicon film 1c is patterned to provide the gate electrode layer 46, "thermal oxidation is conducted . . . to form an oxide film 6e" on the gate electrode layer 46, as illustrated in Figures 3c–3e (all reproduced below). EX1003, 10:42–46. EX1002, ¶79.



EX1003, FIGS. 3c–3e (annotated)

A POSITA would have understood that subjecting the polysilicon gate electrode layer 46 to thermal oxidation would mean that the oxide film 6e is grown by oxidation of the polysilicon gate electrode layer 46, rather than deposited over the polysilicon gate electrode layer 46. *See id.*, Figure 3e. This is also how the '112

patent discloses forming an oxidation layer 68 over the polysilicon gates 38 during an intermediate step in the fabrication of the MOSFET 21. EX1001, 6:20–26 ("an oxidation layer 68 is grown over the entire upper surface of intermediate semiconductor product 58a [by the step of]: Dry oxidation for 6 hrs. at 1000 C …"); *see also id.*, Figure 7. According to *Ueno*, the oxide film 6e is then subjected to etching such that "[t]he polysilicon film 1c remains covered by the thick oxide film 6e." EX1003, 10:48–52. "The oxide film 6e formed on and along the side of the gate electrode layer 46 provides the **interlayer insulating film 49**," as can be seen both the intermediate structure shown in Figure 3e above and in the final structure shown in Figure 3f (reproduced below). *Id.*, 10:59–61. EX1002, ¶80.



EX1003, FIG. 3f (annotated)

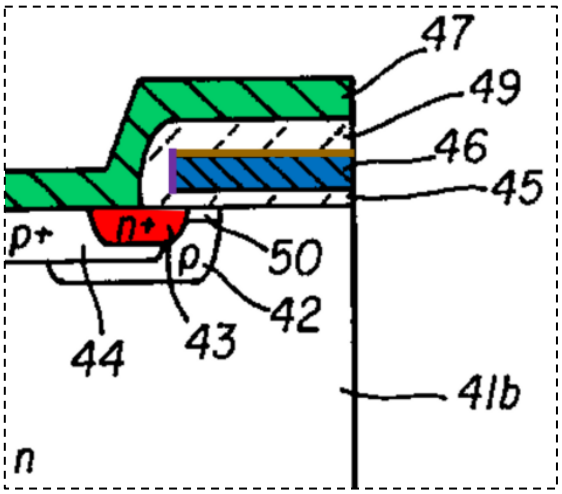
Further, the **interlayer insulating film 49** disclosed in *Ueno* is thicker than the **gate oxide film 45**. Specifically, just as in the '112 patent, *Ueno* explains that the **gate oxide film 45** (*i.e.*, "*a first oxide layer*") is provided by forming an oxide film 6d "by conducting thermal oxidation at 1100°C. for five hours by a pyrogenic method." *Id.*, 10:35–38. *Ueno* states that "[t]he thickness of the **gate oxide film 75**

[*sic*] is ***50 nm***, . . . while the thickness of the **interlayer insulating film 49** is ***2 μm***." *Id.*, 8:29–32. Converting units, 50 nm is equal to 0.05 μm. 2 μm (two microns) is ***forty times*** thicker than 50 nm (fifty nanometers) (*i.e.*, 2 ÷ 0.05 = 40). Therefore, the **interlayer insulating film 49** is thicker than the **gate oxide film 45** (*i.e.*, "*a first oxide layer*") and corresponds to "*a second, thicker oxide layer over said top surface and sidewall of said first gate*." EX1002, ¶81.

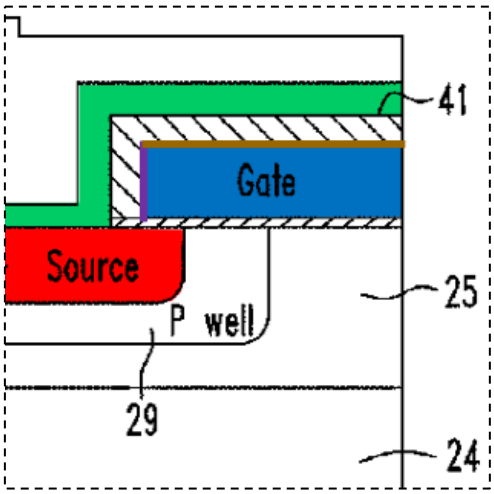
f) 1[e]: "a conformal layer of metal extending laterally across said first gate top surface and sidewall and said adjacent first source region."

Ueno discloses element 1[e]. *Ueno* discloses that a **source electrode 47** (annotated in green below) is formed to be in contact with the n+ **source region 43**. EX1003, 8:10–11 ("A source electrode 47 is formed in contact with both the n+ source region 43 and the p+ well region 44 . . ."). *Ueno* explains that "an ***aluminum alloy*** film is deposited, and patterned, as shown in FIG. 3(f), so as to provide the **source electrode 47** . . ." *Id.*, 10: 62–63. As can be seen in *Ueno*'s excerpted Figure 1 below, the **source electrode 47** conformally and laterally extends across the **top surface** (outlined in brown) and the **sidewall** (outlined in purple) of the right **gate** (*i.e.*, "*said first gate*") and the right **source region 43** (*i.e.*, "*said adjacent first source region*"). This is just as in the '112 patent, as shown below by the side-by-side comparison with the '112 patent's Figure 3. Thus, *Ueno*'s **source electrode 47**

discloses "*a conformal layer of metal extending laterally across said first gate top surface and sidewall and said adjacent first source region*." EX1002, ¶82.



EX1003, FIG. 1
(excerpted and annotated)



EX1001, FIG. 3
(excerpted and annotated)

Just as in the '112 patent, *Ueno*'s **source electrode 47** extends across the **top surface** and the **sidewall** of the right **gate**, and the **gate** is insulated from the **source electrode 47** by an oxide layer. *Cf.* EX1001, Figure 3, 5:1–3 ("polycrystalline silicon (polysilicon) ***gate 38*** that is ***surrounded along*** its top, bottom, left and right sides ***by an insulating layer of silicon dioxide 41***"). Insulating gates from source electrodes by oxide layers was well known in the art. *See*, *e.g.*, EX1009, 15 ("***an oxide layer can be formed over the poly-Si, and the source metallization may then be extended over the whole of the upper surface***"); *id.*, Figure 1.12. EX1002, ¶83.

Therefore, *Ueno* renders obvious claim 1. EX1002, ¶84.

2. Independent Claim 6

a) 6[preamble]: "A MOSFET structure, comprising:"

Regardless of whether the preamble is limiting, *Ueno* discloses it for the same reasons discussed in Section X.A.1.a regarding the preamble of claim 1. EX1002, ¶86.

b) 6[a]: "a silicon carbide wafer having a substrate body with an upper surface, said substrate body having at least one source region formed adjacent said upper surface;"

Ueno discloses element 6[a]. As explained below, *Ueno* discloses a silicon carbide **wafer** having an n drift layer 41b grown on substrate 41a (collectively a "*substrate body*"). EX1003, 8:1–2, 8:54–55 ("the n drift layer 41b . . . is epitaxially grown on the n+ drain layer 41a"). Moreover, *Ueno* has **at least one source region 43** formed adjacent the substrate body's **upper surface**. *Id.*, 8:3–4 ("n+ source region 43"). EX1002, ¶87.

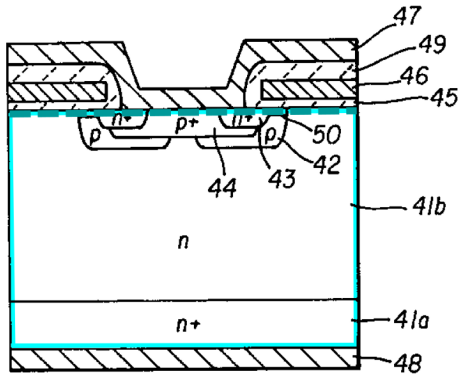
i. 6[a1]: "a silicon carbide wafer"

Ueno discloses element 6[a1] for the same reasons discussed in Section X.A.1.b.i regarding limitation 1[a1]. EX1002, ¶88.

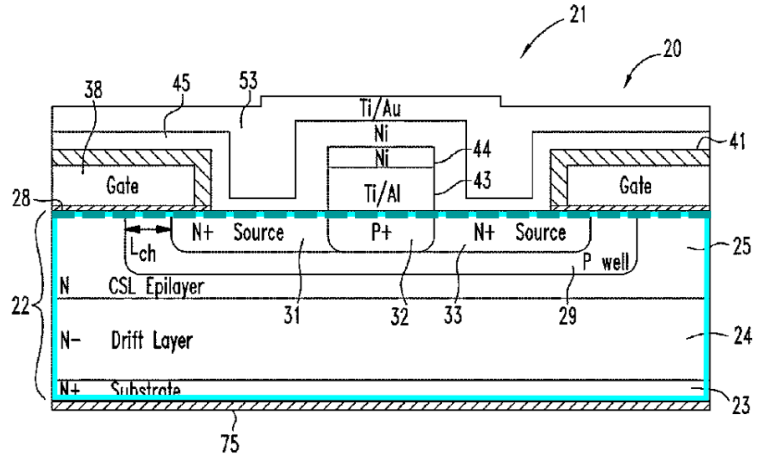
ii. 6[a2]: "having a substrate body with an upper surface"

Ueno discloses element 6[a2]. *Ueno* discloses that, in the **wafer**, "the n drift layer 41b. . . is epitaxially grown on the n+ drain layer 41a." EX1003, 8:1–2, 8:54–55. *Ueno* uses "drain layer" and "substrate" interchangeably to refer to layer 41a.

Id., 8:12–13 ("n+ drain layer or substrate 41a"). The '112 patent refers to its substrate body 22 as the collection of its substrate 23 and overlying layers. EX1001, 4:8–11 ("DMOSFET 21 includes a substrate 23 and a number of semiconductor layers and implants formed on or in the substrate 23 up through top surface 28, ***collectively referred to as the substrate body 22***."); *cf.*, EX1019, ¶4 ("the transistor is formed in a ***body*** 1 ***of semiconductor material comprising*** an N+-type ***substrate*** 2 ***and*** an N−-type ***epitaxial layer*** 3."). In *Ueno*, the substrate 41a and overlying drift layer 41b form its substrate body. Thus, *Ueno*'s **wafer** has a substrate body. Moreover, *Ueno's* substrate body has an **upper surface**, as identified with a dashed teal line, below. *Ueno*'s Figure 1 is reproduced below for comparison with the '112 patent's Figure 3. EX1002, ¶89.



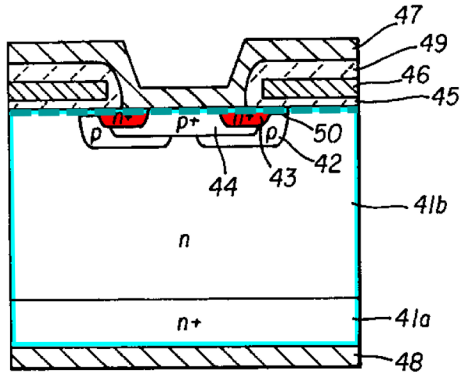
EX1003, FIG. 1 (annotated)



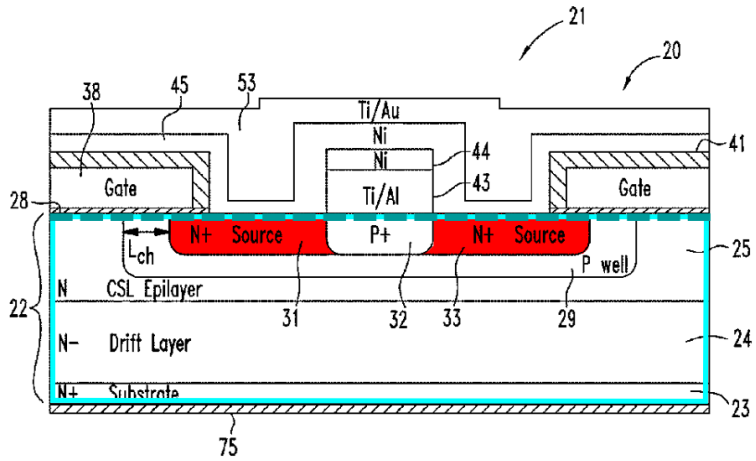
EX1001, FIG. 3 (annotated)

iii. 6[a3]: "said substrate body having at least one source region formed adjacent said upper surface"

Ueno discloses element 6[a2]. As explained below, *Ueno*'s Figure 1 shows the **wafer** having two (*i.e.*, "*at least one*") **source regions 43** (annotated in red below) formed adjacent the **upper surface** of the **wafer**. EX1003, 8:11 ("source region 43"). A side-by-side comparison below with the '112 patent's Figure 3 shows that, in both *Ueno* and the '112 patent, the **source regions** are formed adjacent the **upper surface**. *See also* claim element 1[a2] above. EX1002, ¶90.



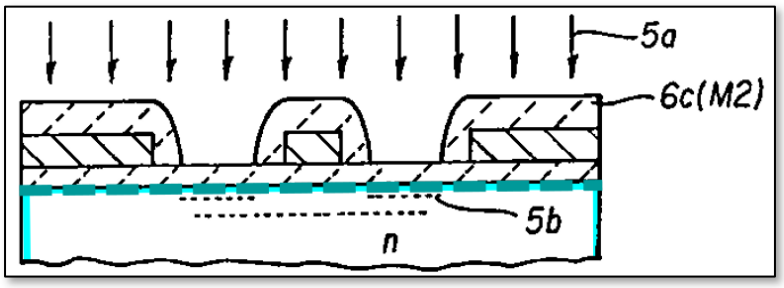
EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

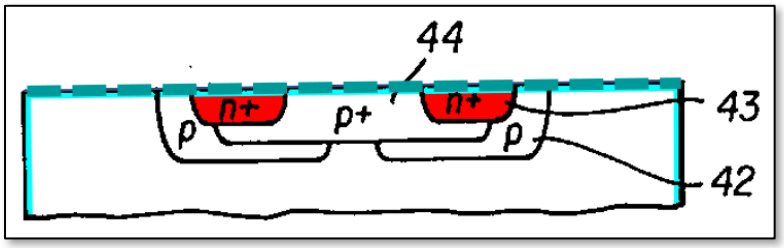
Ueno also discloses the formation of the sources adjacent the upper surface. Specifically, with regard to the process steps for manufacturing the MOSFET of Figure 1, *Ueno* discloses that "nitrogen (N) ions 5a for forming the n+ **source region 43** are implanted" and notes that, in Figure 2g (reproduced below), "reference numeral 5b denotes nitrogen atmos [*sic*] thus implanted." EX1003, 9:59–62, Figure

2g. As can be seen in Figure 2g, the nitrogen atoms 5b are adjacent the **upper surface**. EX1002, ¶91.



EX1003, FIG. 2g (annotated)

Furthermore, *Ueno* discloses that, after a heat treatment to activate implanted impurities, the **source regions 43** are formed as *Ueno* illustrates in Figure 3b (reproduced below). *Id.*, 10:21–24. Indeed, the **source regions 43** are formed adjacent the **upper surface**. EX1002, ¶92.

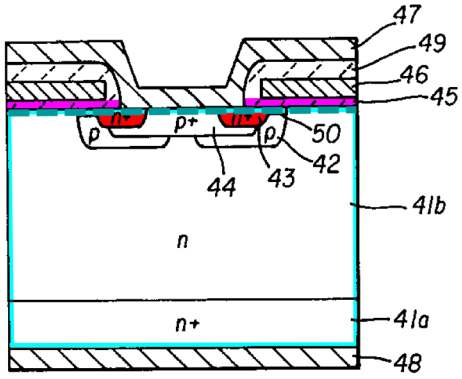


EX1003, FIG. 3b (annotated)

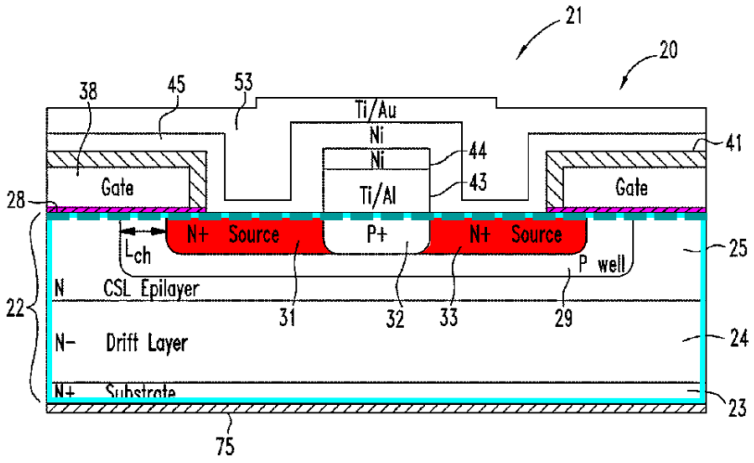
Accordingly, *Ueno* discloses "*said substrate body having at least one source region formed adjacent said upper surface*." EX1002, ¶93.

c) 6[b]: "a substrate surface oxidation layer on said upper surface of said substrate body and adjacent said source region;"

Ueno discloses element 6[b]. As explained below, *Ueno*'s Figure 1 shows a **gate oxide film 45** (annotated in magenta below) (*i.e.*, "*a substrate surface oxidation layer*") on the **upper surface** of the **wafer** and adjacent the **source regions 43**. EX1003, 8:7 ("gate oxide film 45"). In both *Ueno* and the '112 patent, there is an **oxidation layer** on the **upper surface** and adjacent the **source regions**, as shown by the side-by-side comparison below with the '112 patent's Figure 3 where the oxide highlighted in magenta is formed on the **top surface 28**. *See also* claim element 1[c] above. EX1002, ¶94.



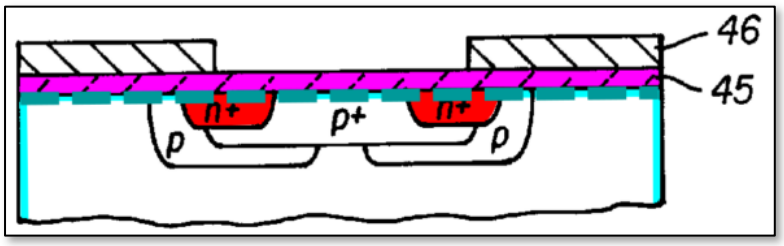
EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

As *Ueno* explains when describing the process steps for manufacturing the MOSFET of Figure 1, "an oxide film 6d . . . provides the **gate oxide film 45**". EX1003, 7:37–39, 10:35–36, Figures 3c and 3d. As can be seen in Figure 3d

(reproduced below), the gate oxide film 45 is on the **upper surface** of the **wafer** and adjacent the **source regions**. EX1002, ¶95.



EX1003, FIG. 3d (annotated)

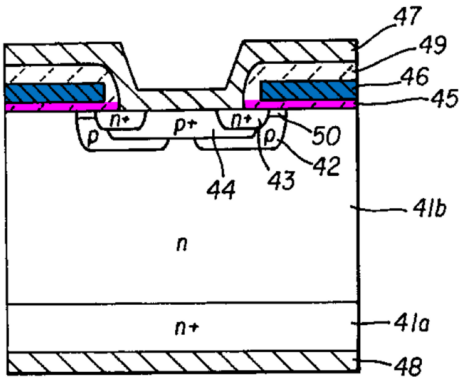
d) 6[c]: "at least two polysilicon gates above said substrate surface oxidation layer, said gates each having a top, a bottom and sides, wherein a first source region of said at least one source region is juxtaposed between first and second adjacent gates of said at least two polysilicon gates;"

Ueno renders obvious element 6[c]. As explained below, *Ueno* explicitly discloses two **gates** that are above the **gate oxide film 45** (*i.e.*, "*said substrate surface oxidation layer*"). EX1003, 8:6–7 ("gate electrode layer 46 made of polysilicon is formed on a gate oxide film 45"). Moreover, each of the two **gates** has a **top**, a **bottom**, and a **side**, as also explained below. As illustrated in *Ueno*'s Figure 1 below, either one of the **source regions 43** is also juxtaposed between the two **gates**. EX1002, ¶96.

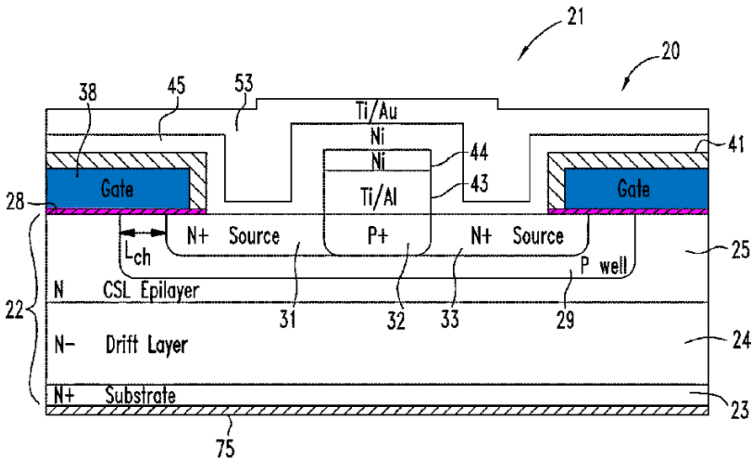
i. 6[c1]: "at least two polysilicon gates above said substrate surface oxidation layer"

Ueno discloses element 6[c1]. For the same reasons discussed in Section X.A.1.c.i regarding limitation 1[b1], *Ueno* discloses two polysilicon **gates**

(annotated in blue below). Further, *Ueno*'s Figure 1 (alongside the '112 patent's Figure 3 for comparison) shows the **gates** above the **gate oxide film 45** (*i.e.*, "*said substrate surface oxidation layer*"). EX1002, ¶97.

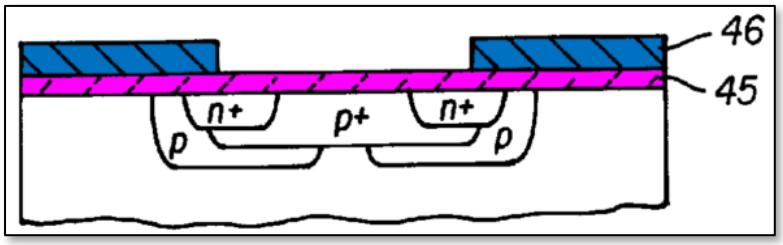


EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

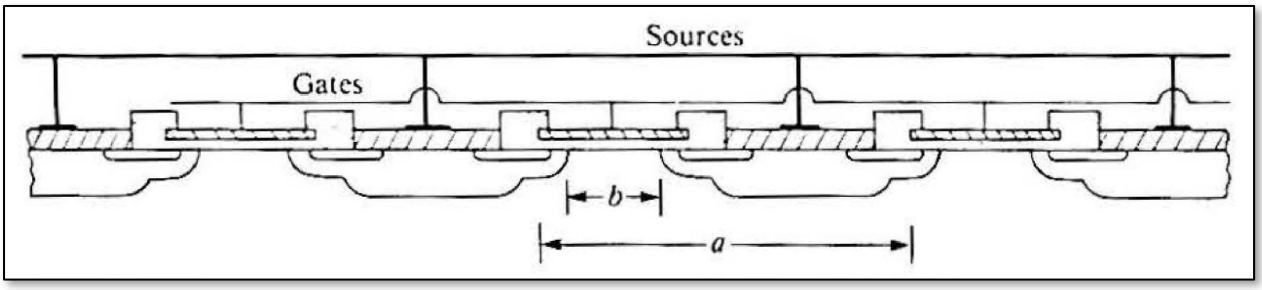
As *Ueno* explains when describing the process steps for manufacturing the MOSFET of Figure 1, a polysilicon film 1c is deposited on the **gate oxide film 45** and patterned to provide the gate electrode layer 46, forming the **gates**. EX1003, 7:37–39, 10:39–44, Figures 3c and 3d. *Ueno*'s Figure 3d (reproduced below) shows the two **gates** above the **gate oxide film 45**. EX1002, ¶98.



EX1003, FIG. 3d (annotated)

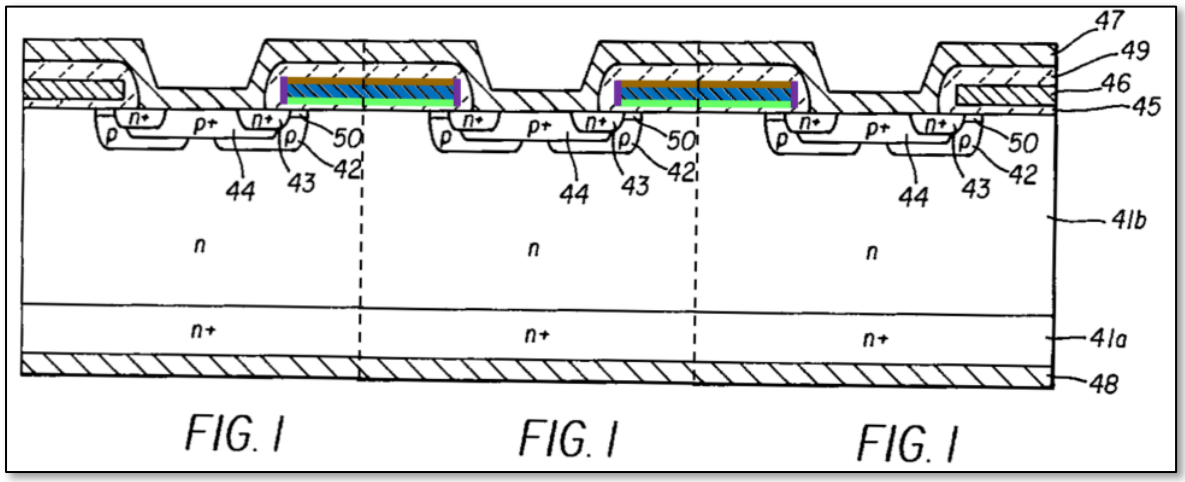
ii. 6[c2]: "said gates each having a top, a bottom and sides"

Ueno renders obvious element 6[c2]. *Ueno* discloses that "FIG. 1 is a cross-sectional view of a unit cell of SiC vertical MOSFET according to one preferred embodiment of the present invention." EX1003, 7:65–67. *Ueno* also discloses that "[t]he pitch of unit cells as shown in FIG. 1 is about 25 μm." EX1003, 8:32–33. A POSITA would have understood *Ueno*'s disclosure that Figure 1 is a "unit cell" and the "pitch of the unit cells" to mean that multiple such unit cells are laid out next to each other spaced apart by the pitch of 25 μm. For example, as discussed in Section VI.C above, *Grant* explains this well-known concept of pitch, stating that "VDMOS FET gates may be laid out as linear arrays, interdigitated with the source, as shown in Figure 3.9*a* . . . where *a* is the pitch of the array." EX1009, 455, Figure 3.9a. *Cf.* EX1001, 4:35–38 ("It should be understood that the semiconductor device (MOSFET 21) of FIG. 3 may be a single 'transistor cell' and that a completely fabricated transistor device may include any number of such semiconductor devices or cells."). An excerpt of *Grant*'s Figure 3.9*a* is reproduced below, illustrating the pitch *a*. EX1009, 70–73, Figure 3.9; *see also id.* at 16, Figure 1.13. EX1002, ¶99.



EX1009, Figure 3.9*a* (excerpted)

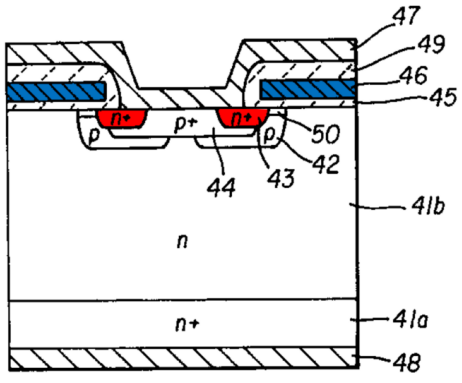
As shown below, multiple copies of *Ueno*'s unit cell of Figure 1 are depicted side by side, per *Ueno*'s teaching of "unit cell" and "pitch of the unit cells" as would be understood by a POSITA and as illustrated and taught by *Grant*. *Ueno* explicitly discloses that each of its two **gates** in Figure 1 has a **top** (outlined in brown) and a **bottom** (outlined in lime). While *Ueno* does not explicitly show both ends of the gates, a POSITA would have recognized, at least in view of *Ueno*'s teachings of unit cells and pitch, that each gate would have had two **sides** (outlined in purple). *See also* claim element 1[b3] above. EX1002, ¶100.



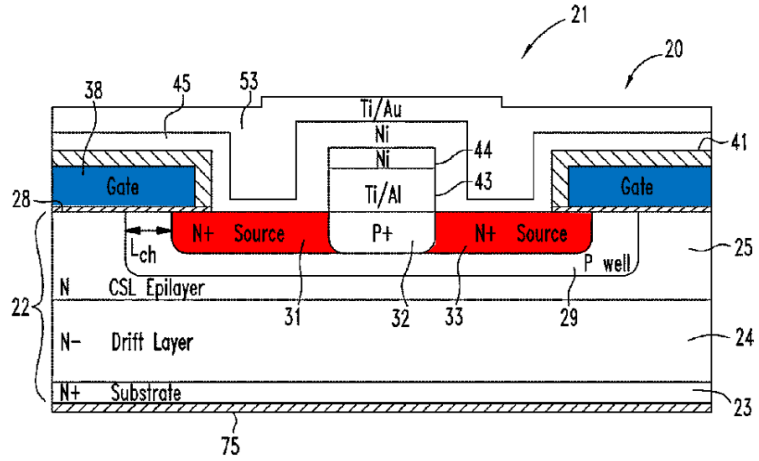
EX1003, FIG. 1 (replicated and annotated)

iii. 6[c3]: "a first source region of said at least one source region is juxtaposed between first and second adjacent gates of said at least two polysilicon gates"

Ueno discloses element 6[c3]. As illustrated in *Ueno*'s Figure 1 below, either one of the **source regions 43** is positioned between (i.e., "*juxtaposed*") the two **gates** 46. EX1003, 8:6–10 ("A ***gate electrode layer 46 made of polysilicon*** is formed on a gate oxide film 45, over the surface of the p base region 42 that is interposed between the ***n^+ source region 43*** and the exposed surface portion of the n drift layer 41b."), 10:21–24, 10:42–44. Because there is no intervening gate between the two **gates**, they are adjacent each other. A side-by-side comparison below with the '112 patent's Figure 3 shows that, in both *Ueno* and the '112 patent, the **source regions** are between the two **gates**. Thus, *Ueno* discloses "*a first source region of said at least one source region is juxtaposed between first and second adjacent gates of said at least two polysilicon gates*." EX1002, ¶101.



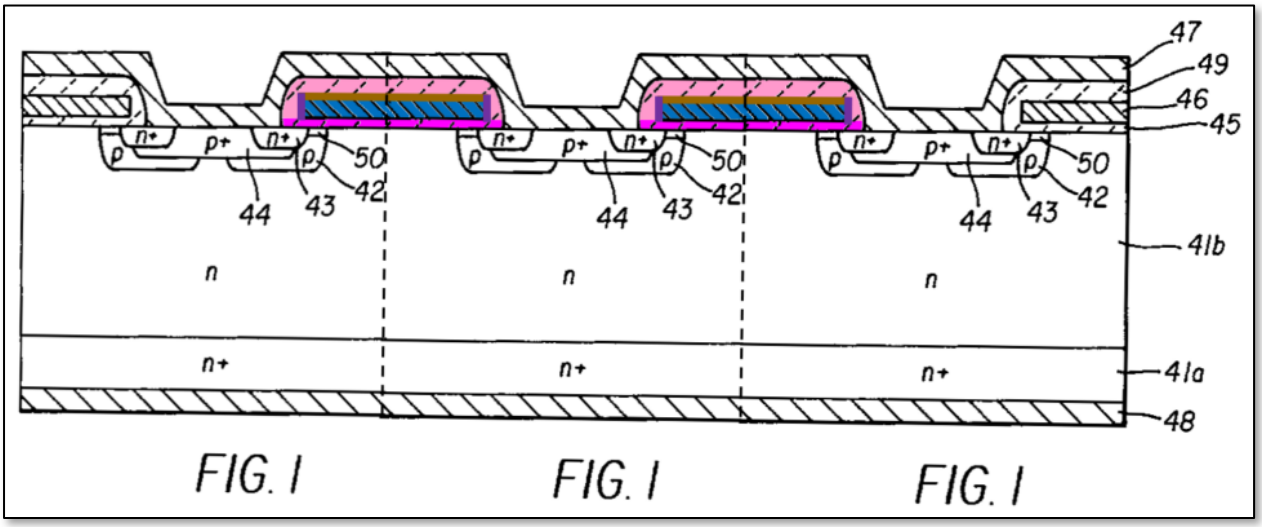
EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

e) 6[d]: "a gate oxide layer, thicker than said substrate surface oxidation layer, over said tops and sides of each of said gates; and"

Ueno discloses element 6[d]. In the one of the process steps for manufacturing the MOSFET of Figure 1, *Ueno* discloses that, after "the oxide film 6e is subjected to wet etching or dry etching," "[t]he oxide film 6e formed ***on and along the side*** of the gate electrode layer 46 provides the **interlayer insulating film 49**" (annotated in pink below). EX1003, 7:37–39, 10:48–61, Figures 3e and 3f. *Ueno*'s replicated and annotated Figure 1 below illustrates the **interlayer insulating film 49** ("*a gate oxide layer*") over the **tops** (outlined in brown) and the **sides** (outlined in purple) of the **gates**. *See also* claim element 1[d] above. EX1002, ¶102.



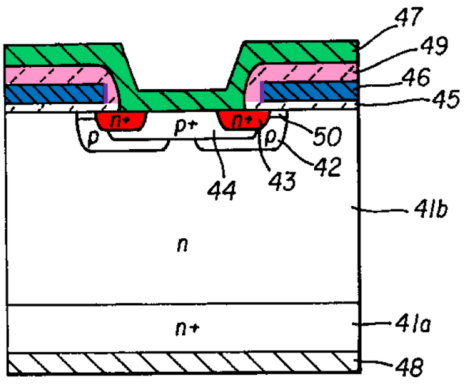
EX1003, FIG. 1 (replicated and annotated)

For the same reasons discussed in Section X.A.1.e regarding limitation 1[d], a POSITA would have understood that the **interlayer insulating film 49** is grown

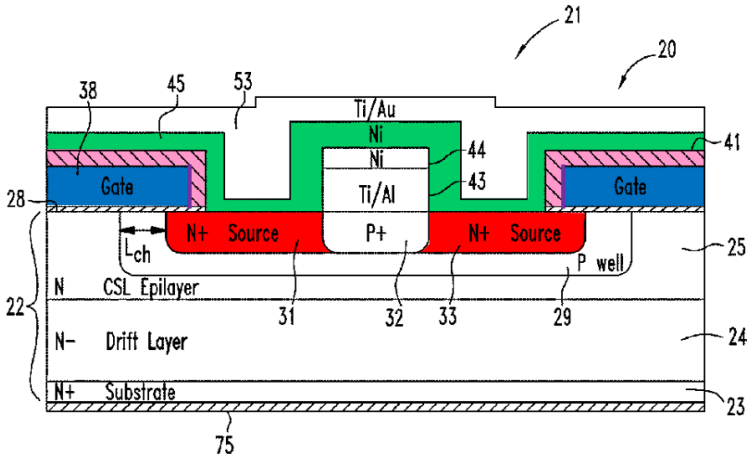
by oxidation of the polysilicon gate electrode layer 46, rather than deposited over the polysilicon gate electrode layer 46, just like the '112 patent discloses forming an oxidation layer 68 over the polysilicon gates 38. Also for those same reasons, the **interlayer insulating film 49** (*i.e.*, the "*gate oxide layer*" in claim 6) is thicker than the **gate oxide film 45** (*i.e.*, the "*substrate surface oxidation layer*" in claim 6). EX1002, ¶103.

f) 6[e]: "a material layer over said first source region and between said gate oxide layers on said sides of said gates, said material layer comprising one of an oxide and a metal contact."

Ueno discloses element 6[e]. For the same reasons discussed in Section X.A.1.f regarding limitation 1[e], *Ueno*'s **source electrode 47** (annotated in green below) is in ***contact*** with the n+ **source region 43** and is made of an ***aluminum alloy*** film. Thus, the **source electrode 47** is a metal contact over and contacting the **source regions 43**. Further, as can be seen in *Ueno*'s Figure 1 below (alongside the '112 patent's Figure 3 for comparison), the **source electrode 47** is between the **interlayer insulating film 49** on the **sides** of the **gates**. *See also* element 1[e] above. EX1002, ¶104.



EX1003, FIG. 1 (annotated)



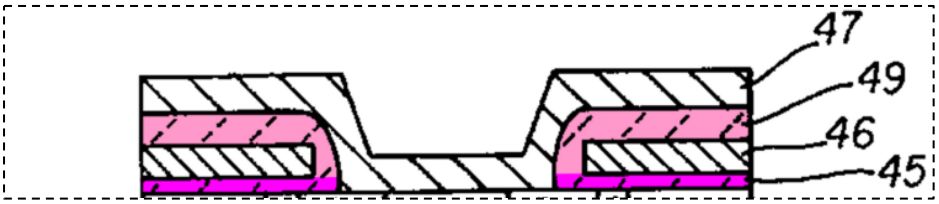
EX1001, FIG. 3 (annotated)

Therefore, *Ueno* renders obvious claim 6. EX1002, ¶105.

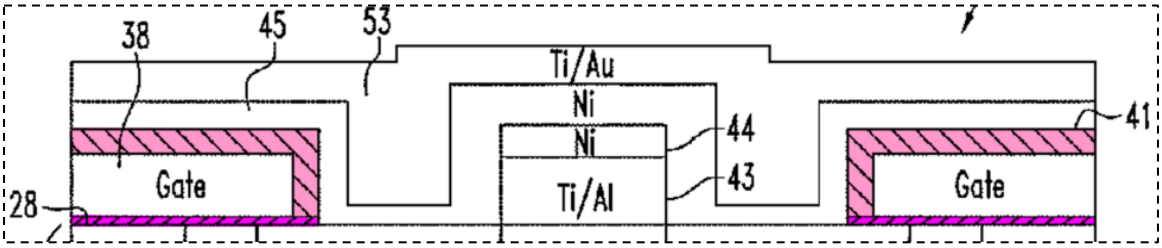
3. Dependent Claim 7

"The MOSFET structure of claim 6, wherein said gate oxide layer is more than eight times thicker than said substrate surface oxidation layer."

Ueno renders obvious claim 6, as discussed above. *Ueno* also discloses "*wherein said gate oxide layer is more than eight times thicker than said substrate surface oxidation layer.*" As discussed above with respect to element 6[d], *Ueno* discloses that "[t]he thickness of the **gate oxide film 75** [*sic*] is ***50 nm***, . . . while the thickness of the **interlayer insulating film 49** is ***2 μm***." EX1003, 8:29–32. Converting units, 50 nm is equal to 0.05 μm. 2 μm (two microns) is forty times thicker than 50 nm (fifty nanometers) (*i.e.*, 2 ÷ 0.05 = 40) (*i.e.*, "*more than eight times thicker*"). Therefore, the **interlayer insulating film 49** is more than eight times thicker than the **gate oxide film 45**. *Ueno*'s Figure 1 and the '112 patent's Figure 3 are annotated below for comparison. EX1002, ¶106.



EX1003, FIG. 1 (excerpted and annotated)



EX1001, FIG. 3 (excerpted and annotated)

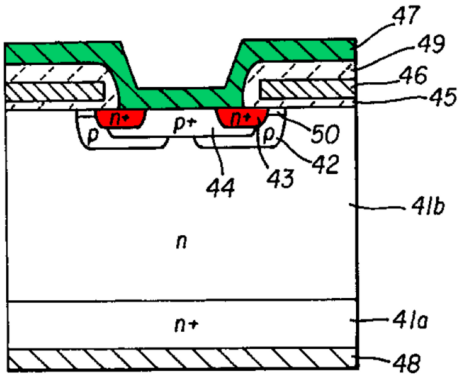
Thus, *Ueno* renders obvious claim 7. EX1002, ¶107.

4. Dependent Claim 10

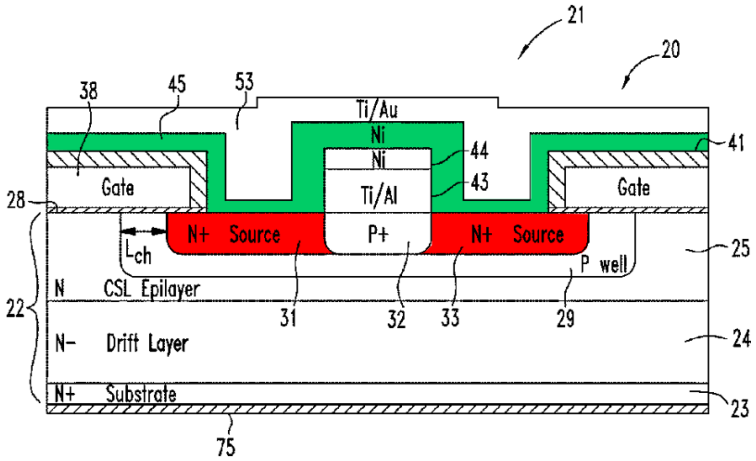
"The MOSFET structure of claim 6, wherein said material layer is a metal contact layer providing external electrical contact with said at least one source region."

Ueno renders obvious claim 6, as discussed above. *Ueno* also discloses "*wherein said material layer is a metal contact layer providing external electrical contact with said at least one source region.*" As discussed above with respect to element 6[e], *Ueno*'s **source electrode 47** is an aluminum contact and is formed to be in ***contact*** with the n+ **source region 43**. EX1003, 8:10–11 ("source electrode 47 is formed to be in contact with both the n+ source 43 and the p+ well region 44"), 10:61–64. *Ueno* describes that, "[w]hen a positive voltage is applied to the gate electrode layer 46, an inversion layer appears in the channel region 50, and current flows between the drain electrode 48 and the source electrode 47 that are now

electrically connected to each other." *Id.*, 8:40–44. A POSITA would have understood that, for current to flow from the drain electrode 48 to the **source electrode 47**—as is the case with MOSFETs during operation—the **source electrode 47** provides external electrical contact because it is the electrode that will be connected to a circuit in which the MOSFET is installed. The circuit is external to the MOSFET itself. *Ueno*'s Figure 1 and the '112 patent's Figure 3 are annotated below side-by-side for comparison. EX1002, ¶108.



EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

Thus, *Ueno* renders obvious claim 10. EX1002, ¶109.

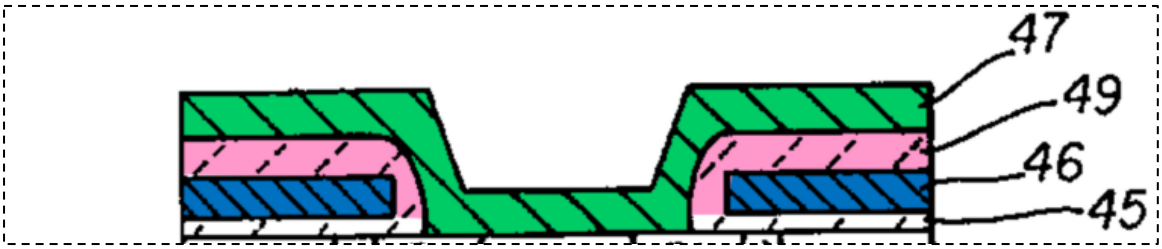
5. Dependent Claim 12

> ***"The MOSFET structure of claim 10, wherein said metal contact layer extends over said gates and covers the space between them, said metal contact layer being in electrical contact with said at least one source region but electrically insulated from said gates by at least one of said gate oxide layer and said substrate surface oxidation layer."***

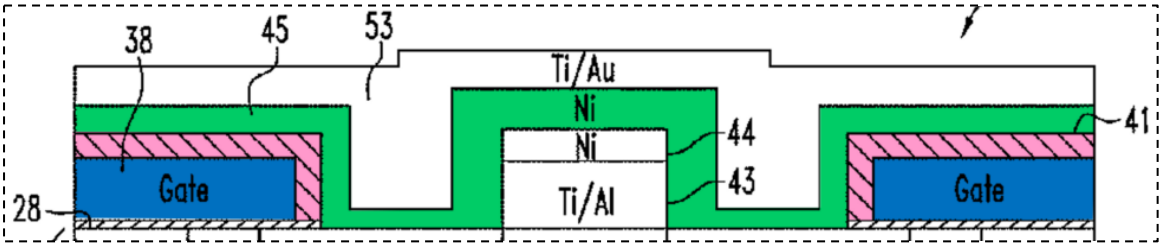
Ueno renders obvious claim 10, as discussed above. As explained below, *Ueno* also discloses "*wherein said metal contact layer extends over said gates and covers the space between them, said metal contact layer being in electrical contact with said at least one source region but electrically insulated from said gates by at least one of said gate oxide layer and said substrate surface oxidation layer.*" EX1002, ¶110.

i. 12[a]: "said metal contact layer extends over said gates and covers the space between them"

Ueno discloses element 12[a]. As discussed above with respect to claim element 6[e] and claim 10, *Ueno*'s **source electrode 47** is a metal contact. Also, *Ueno*'s **source electrode 47** extends over the **gates** and covers the space between the **gates**, as illustrated in the excerpt of Figure 1 below, alongside the '112 patent's Figure 3 for comparison. EX1002, ¶111.



EX1003, FIG. 1 (excerpted and annotated)

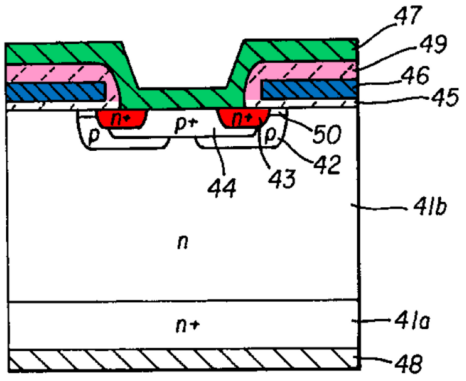


EX1001, FIG. 3 (excerpted and annotated)

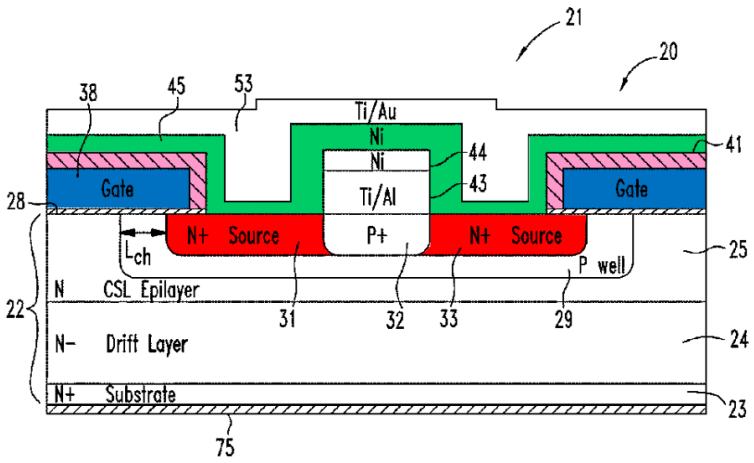
ii. 12[b]: "said metal contact layer being in electrical contact with said at least one source region but electrically insulated from said gates by at least one of said gate oxide layer and said substrate surface oxidation layer"

Ueno discloses element 12[b]. As discussed above with respect to element 6[e] and claim 10, *Ueno*'s **source electrode 47** is a metal contact and is formed to be in ***contact*** with the n+ **source region 43**. EX1003, 8:10–11 ("source electrode 47 is formed to be in contact with both the n+ source 43 and the p+ well region 44"). Also, *Ueno* discloses that "[r]eference numeral 49 denotes an **interlayer insulating film** in the form of a Si oxide film that ***insulates*** the [**gates** provided by] gate electrode layer 46 and the **source electrode 47** from each other." *Id.*, 8:13–16; *see also id.*, Figure 1 (reproduced below alongside the '112 patent's Figure 3). Thus, *Ueno* discloses "*said metal contact layer being in electrical contact with said at least*

one source region but electrically insulated from said gates by at least one of said gate oxide layer and said substrate surface oxidation layer." EX1002, ¶112.



EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

Thus, *Ueno* renders obvious claim 12. EX1002, ¶113.

B. Ground II: Claim 11 is Obvious Over *Ueno* in View of *Lidow*

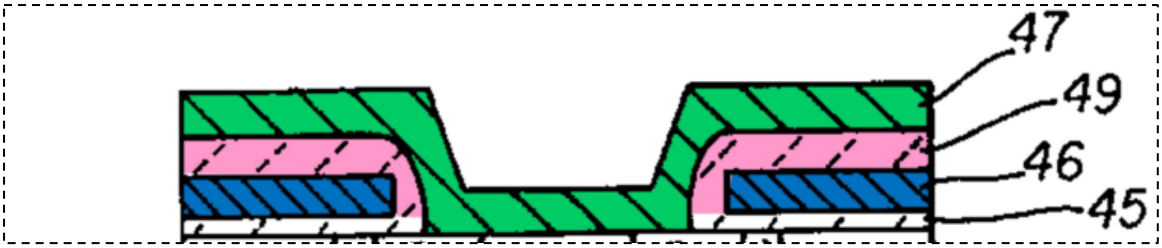
1. Dependent Claim 11

> ***"The MOSFET structure of claim 10 wherein said metal contact layer extends over substantially the entire MOSFET structure except for at least one gate contact access portion, said metal contact layer being in electrical contact with said at least one source region but electrically insulated from said at least two polysilicon gates by at least one of said gate oxide layer and said substrate surface oxidation layer."***

Ueno renders obvious claim 10 as discussed above in Ground I. As explained below, the combination of *Ueno* and *Lidow* renders obvious the limitations of claim 11. EX1002, ¶114.

i. 11[a]: "said metal contact layer extends over substantially the entire MOSFET structure except for at least one gate contact access portion"

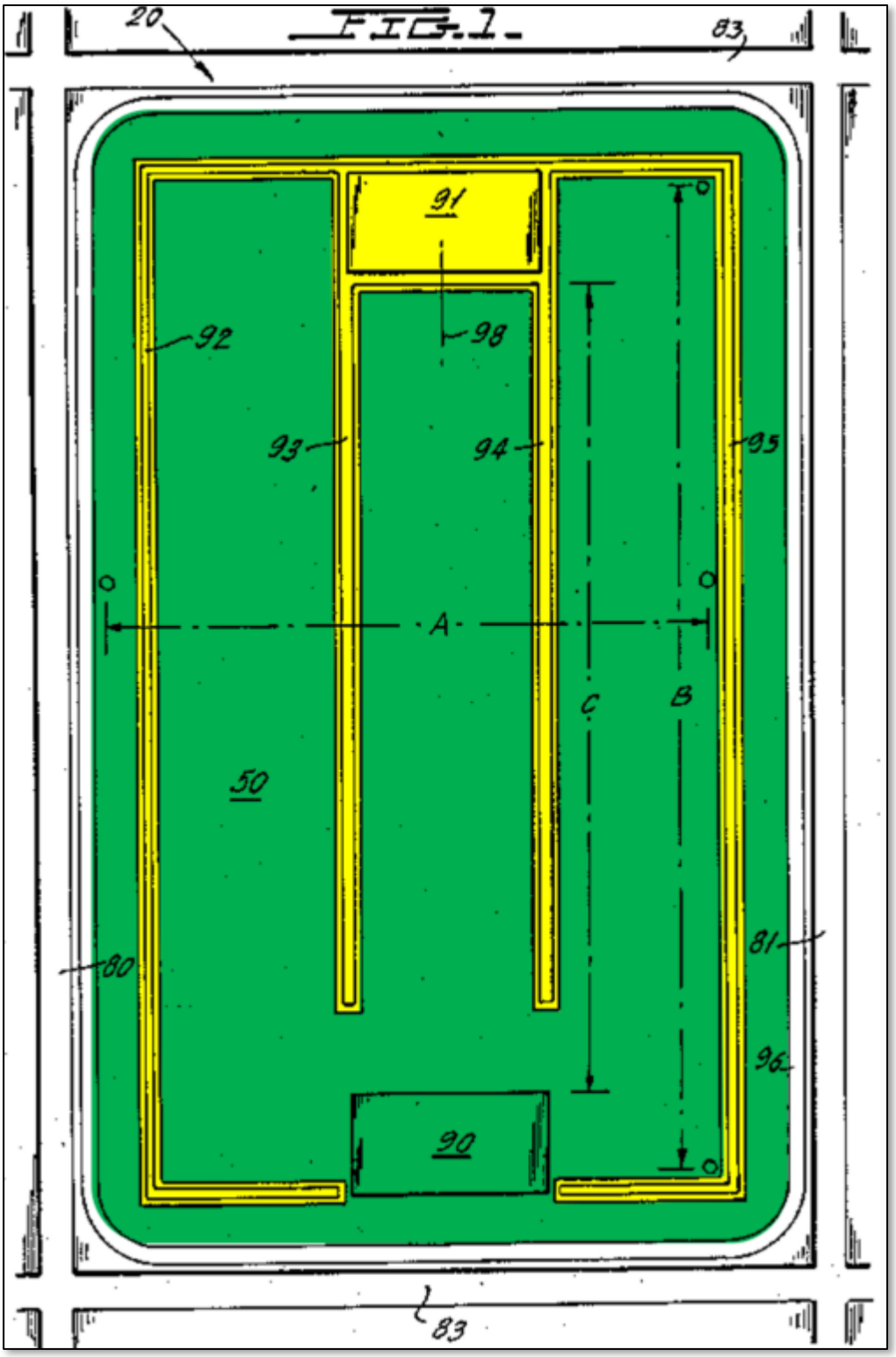
The combination of *Ueno* and *Lidow* renders element 11[a] obvious. As discussed above with respect to claim element 6[e], claim 10, and claim element 12[a], *Ueno*'s **source electrode 47** is a metal contact. *Ueno*'s **source electrode 47** extends over and between the **interlayer insulating film 49** and the **gates**, as illustrated in the excerpt of *Ueno*'s Figure 1 below. EX1002, ¶115.



EX1003, FIG. 1 (excerpted and annotated)

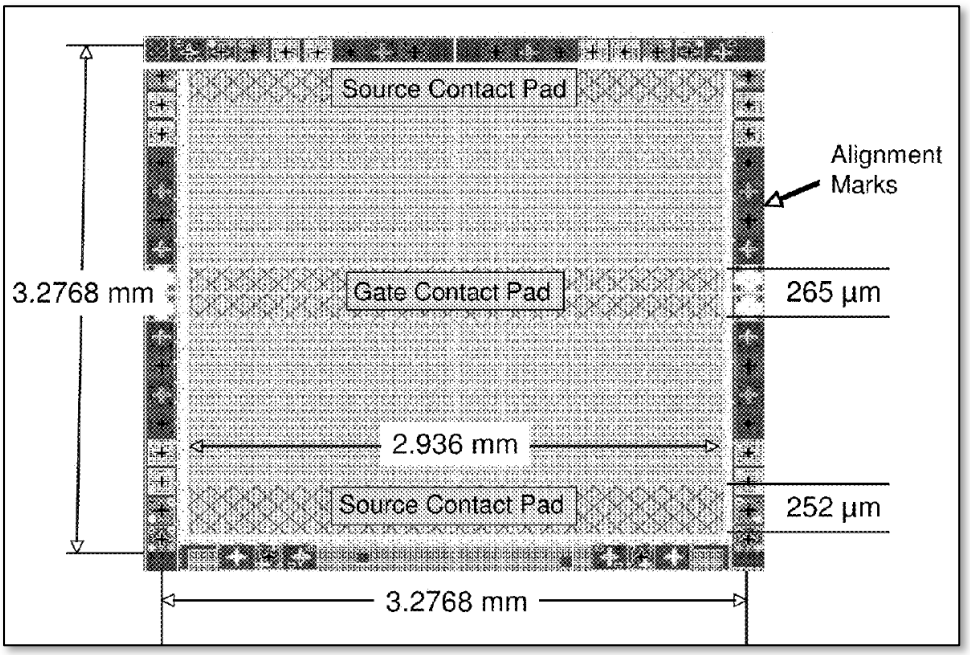
Ueno explains that "an aluminum alloy film is deposited, and patterned, as shown in FIG.3(f), so as to provide the **source electrode 47** and gate electrode (***not illustrated***)." EX1003, 10:61–64. To the extent that *Ueno* does not illustrate that the **source electrode 47** extends over substantially its entire MOSFET structure except for at least one gate contact access portion, *Lidow* does. Specifically, *Lidow* discloses and illustrates in a plan view in Figure 1 (reproduced below) a **source electrode 50** (annotated in green below) that is "deposited over the entire upper surface of the wafer" of a prior-art MOSFET device. EX1014, 5:42–44; *see also id.* 5:44–46 ("the source electrode is shown as conductive coating 50 which may be of

any desired material, such as aluminum"). As can be seen, the **source electrode 50** covers substantially the entire upper surface of the MOSFET device, except for a portion (annotated in yellow) where a "gate connection pad 91 is electrically connected to a plurality of extending fingers 92, 93, 94 and 95 which . . . make electrical connection to the polysilicon gate . . ." *See id.*, 3:21–23, 6:14–19, 6:32–36; *see also id.*, Figure 2. The yellow portion thus provides access to the polysilicon gates. EX1002, ¶116.



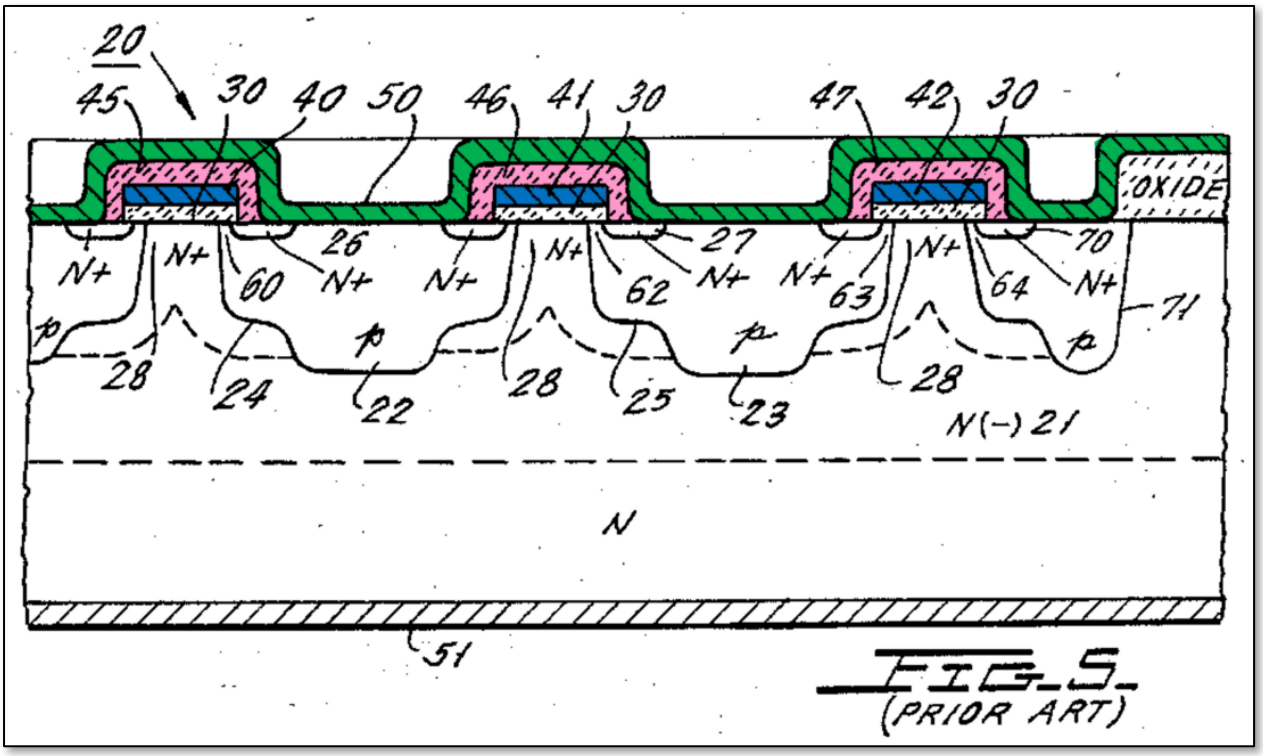
EX1014, FIG. 1 (annotated)

Similar to how *Lidow*'s gate connection pad 91 is used to make electrical connection to the polysilicon gate, the '112 patent describes the use of a "bonding pad for the polysilicon gate" and illustrates a corresponding "Gate Contact Pad" that "runs horizontally across the center of the chip" in a plan view of a MOSFET in Figure 9, reproduced below. EX1001, 2:58–59, 7:37–39. EX1002, ¶117.



EX1001, FIG. 9

Like in *Ueno*, *Lidow*'s **source electrode 50** extends over and between **silicon dioxide coating sections 45, 46, 47** (annotated in pink below) and **polysilicon gates 40, 41, 42** (annotated in blue), as illustrated in *Lidow*'s Figure 5 below. *See id.*, 5:39–41 ("A silicon dioxide coating is then deposited atop the polysilicon grid 40 shown as coating sections 45, 46 and 47 . . ."), 5:37 ("polysilicon sections 40, 41 and 42"), 5:57 ("gate 40"). EX1002, ¶118.



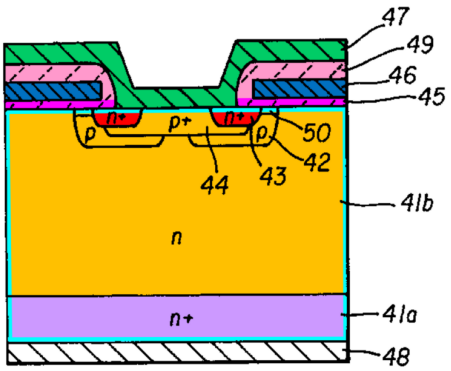
EX1014, FIG. 5 (annotated)

ii. Motivation to Combine Ueno and Lidow

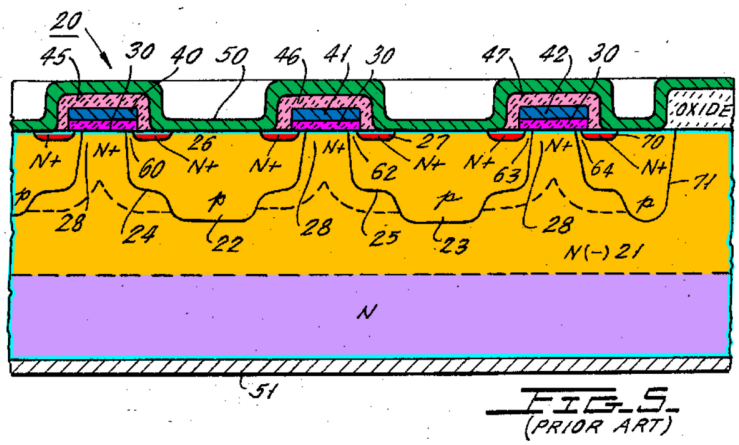
A POSITA would have been motivated to form *Ueno*'s MOSFET according to and informed by *Lidow*'s teachings such that *Ueno*'s **source electrode 47** extends over substantially its entire MOSFET structure except for at least one gate contact access portion, consistent with *Ueno*'s disclosure that a "gate electrode" (*i.e.*, "*gate contact access point*") is provided in its structure when the **source electrode 47** is deposited and patterned. EX1003, 10:61–64 ("After forming the contact hole, an aluminum alloy film is deposited, and patterned, as shown in FIG.3(f), so as to provide the source electrode 47 and ***gate electrode*** (not illustrated)."). EX1002, ¶119.

Ueno and *Lidow* are from the same field of endeavor. *See, e.g.*, *Medtronic, Inc. v. Cardiac Pacemakers, Inc.*, 721 F.2d 1563, 1574–75 (Fed. Cir. 1983); M.P.E.P. § 2141. Both references are directed to power MOSFETs. *Ueno* discloses "a method for manufacturing silicon carbide vertical MOS semiconductor devices having high breakdown voltage." EX1003, 4:45–46. *Lidow* discloses "a novel configuration for the central high conductivity region disposed beneath the gate oxide of a high power MOSFET." EX1014, 1:23–25. Thus, both references are directed to power MOSFETs and aim at improving their characteristics. EX1002, ¶120.

Although *Ueno* is directed to silicon-carbide MOSFETs and *Lidow* to silicon MOSFETs, *Baliga* teaches that conventional power MOSFETs, including silicon MOSFETs, "can be readily translated into silicon carbide using known manufacturing techniques." EX1004, 4:22–38. *Ghezzo* also teaches a method of replacing the conventional double-diffusion used in silicon MOSFETs with a double ion implantation sequence for SiC MOSFETs. EX1010, 1:56–63. Moreover, *Ueno*'s MOSFET and *Lidow*'s prior-art MOSFET share the same relevant semiconductor structure and features, as can be seen by the side-by-side comparison below. Accordingly, a POSITA would have understood that the teachings of *Lidow* were directly applicable to *Ueno*'s SiC MOSFETs. EX1002, ¶121.



EX1003, FIG. 1 (annotated)



EX1014, FIG. 5 (annotated)

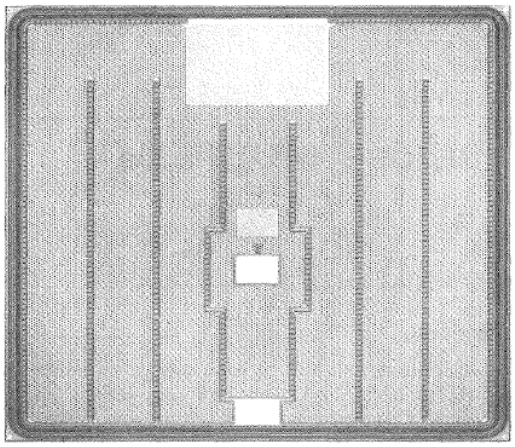
Implementing *Ueno*'s **source electrode 47** such that it extends over substantially *Ueno*'s entire MOSFET structure except for *Ueno*'s disclosed, but not illustrated, "gate electrode" in the manner shown by *Lidow* would have yielded expected, predictable results. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007); M.P.E.P. 2143(I)(A). *Ueno* discloses its **source electrode 47** extending over and between **interlayer insulating film 49** and **gates**. EX1003, Figure 1. *Ueno* also explains that a "gate electrode" is provided in its structure when the **source electrode 47** is deposited and patterned. EX1003, 10:61–64; *see also, id.*, 1:40–42, 57–59 (explaining in a "unit cell of typical Si vertical MOSFET that has been generally used as a power semiconductor device" that a "gate electrode made of metal is held in contact with the gate electrode layer 16 at a portion that is not illustrated in the figure."). EX1002, ¶122.

Similarly, *Lidow* discloses its **source electrode 50** extending over and between **silicon dioxide coating sections 45, 46, 47** and **polysilicon gates 40, 41,**

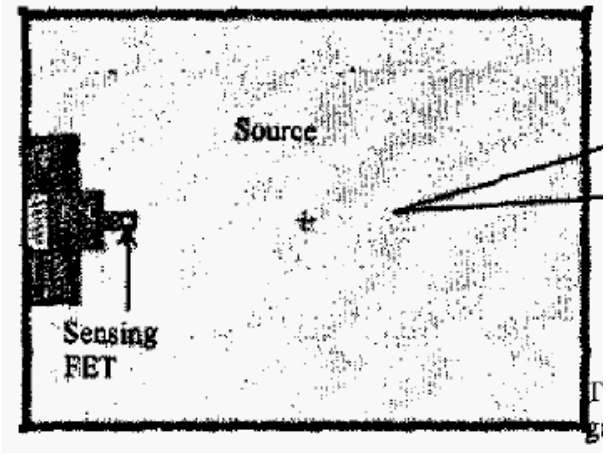
42. EX1014, Figure 5. *Lidow* further illustrates **source electrode 50** covering substantially the entire upper surface of the MOSFET device, except for a portion where a "gate connection pad 91 is electrically connected to a plurality of extending fingers 92, 93, 94 and 95 which . . . make electrical connection to the polysilicon gate . . ." *See id.*, Figure 1, 3:21–23, 6:14–19, 6:32–36; *see also id.*, Figure 2. Because *Ueno* does not illustrate its gate electrode, a POSITA would have been motivated to look to references like *Lidow* that do illustrate the gate electrode. A POSITA would have used the disclosures of *Ueno* and *Lidow*—namely, the **source electrode 47** extending over and between **interlayer insulating film 49** and **gates** as taught by *Ueno*, and the **source electrode 50** covering substantially the entire upper surface of the MOSFET device, except for a portion providing access to **polysilicon gates** as taught by *Lidow*—using known and routine semiconductor fabrication techniques to form *Ueno*'s **source electrode 47** such that it extends over substantially *Ueno*'s entire MOSFET structure except for at least one gate contact access portion to provide *Ueno*'s "gate electrode." EX1002, ¶123.

Moreover, a POSITA would not have been deterred by *Ueno*'s absence of illustrations of the gate electrode because such structures were notoriously well known as shown by *Lidow* as well as many other references. For example, *Grant* illustrates such an arrangement in Figure 19.1 (reproduced below), where in a "current-sensing MOSFET die… the gate pad is at the bottom." EX1009, 384.

Similarly, *Xiao* shows "the top view of die layout and cell geometry" of a MOSFET where the "[m]ajority area of the die is covered with source metallization of switching FET, ***except the bonding pads for gate (G)*** . . ." EX1018, 767, Figure 3 (reproduced below); *see also* EX1020, 2:22–26, 4:14–22, Figure 7 (reproduced below, illustrating source contact metallization 31 covering substantially the entire top surface of a complete vertical FET except for interconnection metallization 35 that makes connection to all gate regions and to gate contact pad 36). EX1002, ¶124.



EX1009, FIG. 19.1 (excerpted)



EX1018, FIG. 3 (excerpted)

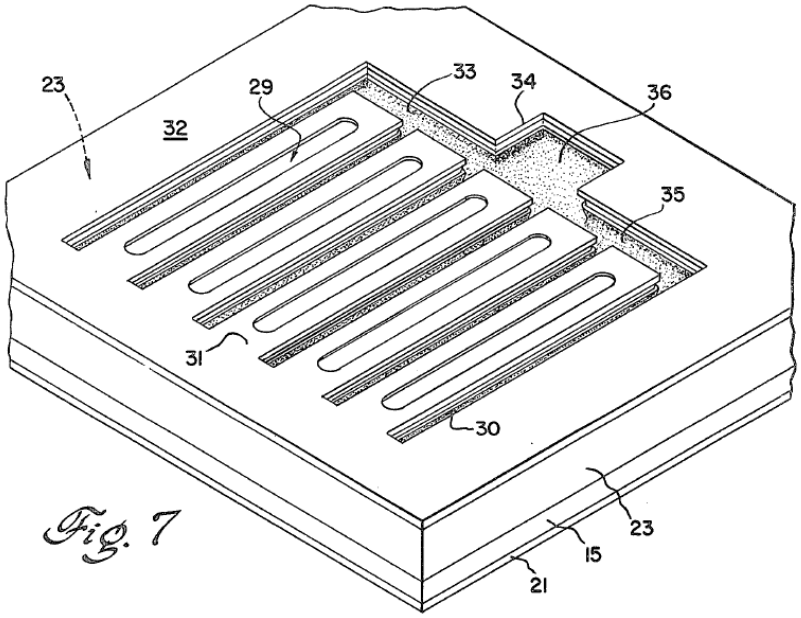


Fig. 7

EX1020, FIG. 7

This result would have been readily predictable and recognized by a POSITA because, as *Lidow* teaches, extending the source electrode over substantially the entire MOSFET structure except for a gate contact access portion would allow for a source pad that facilitates lead connection for the source and a gate pad for lead connection for the gate. *See* EX1014, 6:29–32 ("The source pad 90 is a relatively heavy metal section which is directly connected to the aluminum source electrode 50 and permits convenient lead connection for the source."), 13:8–9 ("Suitable electrode wires are then connected to the source and gate pads . . ."). As shown immediately above, *Lidow*'s arrangement is well-known technique in the field for providing a gate contact in a MOSFET die. *See, e.g.*, EX1009, 384, Figure 19.1; EX1018, 767, Figure 3; EX1020, 2: 22–26, 4:14–22, Figure 7. EX1002, ¶125.

A POSITA would have been further motivated to combine the teachings of *Ueno* and *Lidow* because it would have simply provided the simple substitution of one known element (**source electrode 47** extending over and between **interlayer insulating film 49** and **gates** in *Ueno*) for another (**source electrode 50** covering substantially the entire upper surface of the MOSFET device, except for a portion providing access to **polysilicon gates** as taught by *Lidow*) to obtain predictable results. *KSR*, 550 U.S., 416; M.P.E.P. 2143(I)(B). This substitution would have been readily achievable by a POSITA via known and routine semiconductor fabrication techniques to implement *Ueno*'s **source electrode 47** such that it extends over substantially *Ueno*'s entire MOSFET structure except for at least one gate contact access portion to provide *Ueno's* "gate electrode." EX1002, ¶126.

Forming *Ueno*'s **source electrode 47** in the same manner as *Lidow*'s **source electrode 50** would have been readily implemented by simply modifying the masks used to form *Ueno*'s **source electrode 47**. A POSITA could have achieved this implementation using basic semiconductor fabrication techniques to modify *Ueno*'s **source electrode 47** such that it extends over substantially *Ueno*'s entire MOSFET structure except for at least one gate contact access portion as identified by *Ueno* and shown by *Lidow*. This implementation would have been well within the knowledge and skillset of a POSITA. EX1002, ¶127.

iii. Reasonable Expectation of Success in Combining Ueno and Lidow

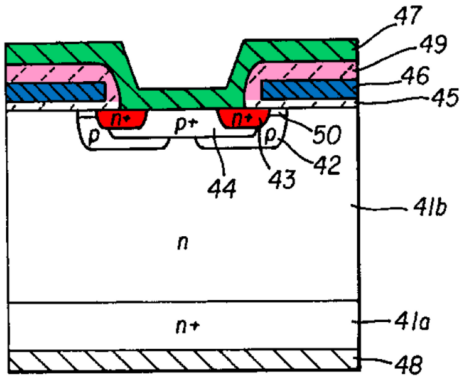
A POSITA would also have had a reasonable expectation of success. The combination of *Ueno* and *Lidow* represents a straight-forward implementation of steps of the well-understood semiconductor fabrication processes to implement the shape and location of the structures, which a POSITA would have been familiar with and been able to implement. The reasons a POSITA would have expected success parallel those that provide motivation for this combination—including because both *Ueno* and *Lidow* are directed to vertical power MOSFETs. EX1003, 4:45–46, Figure 1; EX1014, 1:23–25, Figures 1–5. A POSITA would have had a reasonable expectation of success in implementing *Ueno*'s MOSFET electrodes per the teachings of *Lidow* because *Ueno*'s underlying specification was designed to be extensible and flexible. Indeed, *Ueno* did not provide details of how to implement its gate electrode because such structures were well known as illustrated by *Lidow* as well as many other references. *See, e.g.*, EX1009, 384, Figure 19.1; EX1018, 767, Figure 3; EX1020, 2: 22–26, 4:14–22, Figure 7. EX1002, ¶128.

Accordingly, *Ueno* in view of *Lidow* renders obvious element 11[a] and a POSITA would have been motivated to combine the teachings of these references and would have had a reasonable expectation of success. EX1002, ¶129.

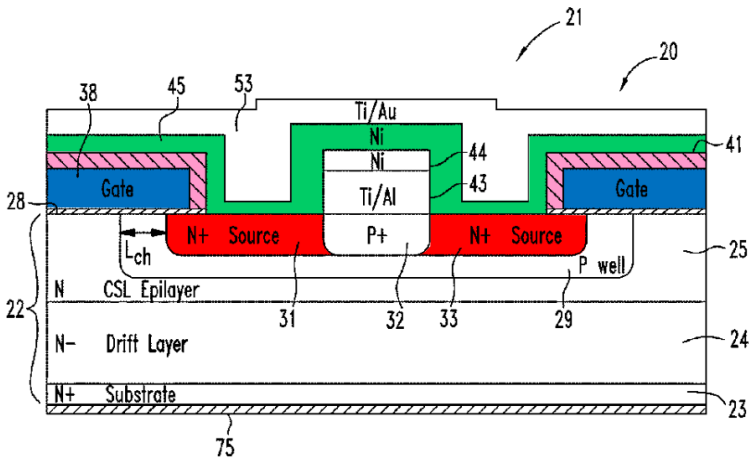
iv. 11[b]: "said metal contact layer being in electrical contact with said at least one source region but

electrically insulated from said at least two polysilicon gates by at least one of said gate oxide layer and said substrate surface oxidation layer"

Ueno discloses element 11[b]. As discussed above with respect to element 6[e] and claim 10, *Ueno*'s **source electrode 47** is a metal contact and is formed to be in ***contact*** with the n+ **source region 43**. EX1003, 8:10–11 ("source electrode 47 is formed to be in contact with both the n+ source 43 and the p+ well region 44"). *Ueno* discloses that "[r]eference numeral 49 denotes an **interlayer insulating film** in the form of a Si oxide film that ***insulates*** the [two **gates** formed by] gate electrode layer 46 and the **source electrode 47** from each other." *Id.*, 8:13–16; *see also id.*, Figure 1 (reproduced below alongside the '112 patent's Figure 3). EX1002, ¶¶130-131.



EX1003, FIG. 1 (annotated)



EX1001, FIG. 3 (annotated)

Therefore, *Ueno* discloses "*said metal contact layer being in electrical contact with said at least one source region but electrically insulated from said at*

least two polysilicon gates by at least one of said gate oxide layer and said substrate surface oxidation layer." EX1002, ¶132.

Thus, *Ueno* in view of *Lidow* renders obvious claim 11. EX1002, ¶133.

XI. CO-PENDING DISTRICT COURT LITIGATION IN TEXAS SHOULD NOT PRECLUDE INSTITUTION

Although there is concurrent district court litigation involving the '112 patent, the weight of the factors described in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 5–6 (PTAB Mar. 20, 2020) (precedential) favors institution of this Petition.

A. The potential for a stay of the district court case urges against denial (factor 1)

After any institution of review based on this Petition, ST intends to seek a stay of the co-pending district court proceedings. Therefore, factor 1 is neutral because any decision by the district court to stay the case would issue after institution and be based on "a variety of circumstances and facts beyond [the Board's] control and to which the Board is not privy." *See Sand Revolution II, LLC v. Cont'l Intermodal Grp. Trucking, LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative).

B. Uncertainty over the trial date in the Texas case favors institution (factor 2)

The district court recently entered a Scheduling Order identifying April 24, 2023 as the target trial date. EX1015, 5. Based on the expected 18-month IPR

schedule, a final written decision (FWD) in this proceeding would likely issue by June 2023—within less than two months of the court's initial target date for trial.

The close proximity between the district court's target trial date and the Board's FWD date favors institution, or is neutral, because the district court's trial date is subject to considerable uncertainty. *Sand Revolution*, IPR2019-01393, Paper 24 at 9-10 (uncertainty of trial date weighed in favor of institution) (informative); *Micron Tech., Inc. v. Godo Kaisha IP Bridge 1*, IPR2020-01008, Paper 10 at 14 (PTAB Dec. 7, 2020) ("due to the uncertainty as to this trial date, this factor is, at most, neutral").

Despite the district court's aspirational target date, trial is unlikely to begin on April 24, 2023 and may be postponed until after the Board issues a FWD in this proceeding. Delays may result from (i) the continued impact of and uncertainty surrounding the COVID-19 pandemic, (ii) the court's crowded docket, which currently includes at least 802 pending patent cases (EX1016), and (iii) the tendency for trial dates in the Western District of Texas to slip from the court's initial target dates—EX1017, 3 ("In the WDTX, 70% of trial dates initially relied upon by the PTAB to deny petitions have slid.").

In contrast to the potential delays to the district court's schedule, the Board's schedule is unlikely to shift. Barring exceptional circumstances, the Board must issue its FWD within the one-year statutory deadline described in 35 U.S.C.

§ 316(a)(11). *Sand Revolution*, IPR2019-01393, Paper 24 at 9. Further, the Board has remained fully operational despite the challenges presented by COVID-19. *Id.* Given the circumstances, the Board may well issue a FWD before the beginning of any trial in the district court.

Factor 2 also favors institution because ST diligently filed this Petition ***seven months*** before its statutory deadline for doing so. *See, e.g.*, *Apple Inc. v. Seven Networks, LLC*, IPR2020-00156, Paper 10 at 9 & n.8 (PTAB June 15, 2020) (considering the filing date relative to potential filing dates helps to analyze factor 2 on a sliding scale based on relative trial dates).

C. Investment in the parallel district court proceeding is minimal and ST was diligent in filing this Petition (factor 3)

The co-pending district court case is still in an early phase. The court has not addressed the merits of the case. All significant stages of litigation—including discovery, claim construction, summary judgment, and trial—remain in the future. The target trial date is over 15 months away and will likely be delayed. After receiving any institution decision, ST intends to move for a stay in the district court to further minimize investment by the court and the parties. Moreover, ST was diligent in filing this Petition over ***seven months*** before its statutory bar date. *See Seven Networks*, IPR2020-00156, Paper 10 at 11 (filing petition four months before § 315(b) bar date shows diligence).

D. The Petition raises unique issues, which favors institution (factor 4)

ST expects its invalidity positions in the district court case will diverge from the ground of unpatentability described in this Petition. In any event, ST reserves the right to enter a stipulation relating to the district court case that would prevent and/or reduce overlap with the requested IPR, should the Board deem one necessary. Such a stipulation would mitigate concerns about duplicative efforts in the district court case and this IPR proceeding. *See Sand Revolution*, IPR2019-01393, Paper 24 at 12.

E. The parties overlap (factor 5)

The district court case and the IPR proceeding involve the same parties.

F. The merits of ST's challenge support institution (factor 6)

"[I]f the merits of a ground raised in the petition seem particularly strong on the preliminary record … the institution of a trial may serve the interest of overall system efficiency and integrity….". *Fintiv*, IPR2020-00019, Paper 11 at 14–15. As described above, *Ueno* renders obvious the allegedly inventive features of the '112 patent, including the configuration recited by claims 1, 6, 7, 10, and 12, and the combination of *Ueno* and *Lidow* renders obvious claim 11. The merits of the prior art and their close correspondence to the challenged claims favors institution.

XII. CONCLUSION

Petitioner requests institution of an *inter partes* review of the '112 patent and cancellation of claims 1, 6, 7, and 10–12.

Respectfully Submitted,

Dated: December 17, 2021

/Richard Goldenberg/
Richard Goldenberg, Lead Counsel
Registration No. 38,895

TABLE OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 8,035,112
1002	Declaration of Dr. Vivek Subramanian
1003	U.S. Patent No. 6,238,980 ("*Ueno*")
1004	U.S. Patent No. 5,233,215 ("*Baliga*")
1005	'112 Patent File History, 11/12/2010 Preliminary Amendment
1006	'112 Patent File History, 2/23/2011 Non-Final Office Action
1007	'112 Patent File History, 5/23/2011 Response to Office Action
1008	'112 Patent File History, 6/29/2011 Notice of Allowance
1009	D. A. Grant and J. Gowar, "Power MOSFETs – Theory and Applications," 1989 ("*Grant*") (relevant sections)
1010	U.S. Patent No. 5,510,281 ("*Ghezzo*")
1011	J. A. Cooper, Jr. et al., "Status and Prospects for SiC Power MOSFETs," IEEE Transactions on Electron Devices, vol. 49, no. 4, April 2002
1012	J. A. Cooper, Jr. et al., "SiC Power-Switching Devices—The Second Electronics Revolution?," Proceedings of the IEEE, vol. 90, no. 6, June 2002
1013	U.S. Patent No. 5,317,184 ("*Rexer*")
1014	U.S. Patent No. 4,593,302 ("*Lidow*")

Exhibit	Description
1015	Scheduling Order, *The Trustees of Purdue University v. STMicroelectronics, Inc. et al.*, No. 6:21-cv-00727 (W.D. Tex.), Dkt. 45 (November 22, 2021)
1016	Statistics from Docket Navigator showing active patent cases before Judge Alan Albright of the U.S. District Court for the Western Digital of Texas (as of December 17, 2021)
1017	Article entitled "District Court Trial Dates Tend to Slip After PTAB Discretionary Denials" (July 24, 2020)
1018	Y. Xiao et al., "Current Sensing Trench Power MOSFET for Automotive Applications," Twentieth Annual IEEE Applied Power Electronics Conference and Exposition, 2005
1019	U.S. Patent Publication No. 2004/0222483
1020	U.S. Patent No. 4,343,015
1021	P. G. Neudeck, "Progress in Silicon Carbide Semiconductor Electronics Technology," Journal of Electronic Materials, vol. 24, no. 4, 1995
1022	P. Van Zant, "Microchip Fabrication – A Practical Guide to Semiconductor Processing," 1997 (relevant sections)
1023	M. Quirk, et al. "Semiconductor Manufacturing Technology," 2001 (relevant sections)

CERTIFICATE UNDER 37 CFR § 42.24(d)

Under the provisions of 37 CFR § 42.24(d), the undersigned hereby certifies that the word count for the foregoing Petition for *Inter Partes* Review totals 13,797, which is less than the 14,000 words allowed under 37 CFR § 42.24(a)(1)(i).

Respectfully submitted,

Dated: December 17, 2021

/Scott Bertulli/
Scott Bertulli
Reg. No. 75,886

CERTIFICATE OF SERVICE

I hereby certify that on December 17, 2021, I caused a true and correct copy of the foregoing materials:

- Petition for *Inter Partes* Review of U.S. Patent No. 8,035,112 under 35 U.S.C. § 312 and 37 C.F.R. § 42.104
- Exhibit List
- Exhibits for Petition for *Inter Partes* Review of U.S. Patent No. 8,035,112 (EX1001–EX1023)
- Power of Attorney
- Fee Authorization
- Word Count Certification Under 37 CFR § 42.24(d)

to be served via Express Mail on the following correspondent of record as listed on PAIR:

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DATED: December 17, 2021

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